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**Physical Modeling and Reliability Mechanisms in High Voltage
AlGaN/GaN HFETs**

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Final Report**

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14. ABSTRACT The effect of LO phonon lifetime in GaN on the carrier velocity and heterojunction field effect transistor speed and stability has been established. The observed dependence of the LO phonon lifetime on the bulk carrier density has been phenomenologically ascribed to LO phonon-Plasmon interaction with the resonance giving rise to the shortest lifetime and best performance. Specifically, the electron velocity is the highest, as determined by an extraction method using the current gain cut off frequency data in FETs, the stability is the best in charge pumping experiments, the defect generation in the least as probed by low frequency noise measurements. In aggregate, the cumulative data clearly point to the benefits of operation at or near resonance of LO phonon frequency and Plasmon frequency.						
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Final Report

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Abstract

Electrons in many high performance semiconductor based heterostructure devices get hot in relation to the lattice temperature due to acceleration by the electric field, as in the case of field effect transistors or injection into a lower energy region of the structure such as quantum wells as in the case of light emitting diodes and lasers, heterojunction bipolar transistors. The FET case is established and widely known. However, the LED and laser case, although it is straightforward, is not as established as it should be, luckily demonstrated by our group recently. In highly ionic semiconductors, a case in point is GaN, electron phonon coupling is very strong which causes high rate of generation of LO phonons. Unfortunately, LO phonons lack group velocity and accumulate. Unless they decay to LA phonons which can traverse the semiconductor relatively efficiently, they cause local heating and act as scatterers for electrons, both to the detriment of the device in hand.

In this reporting period, we firmly established that the hot LO phonon decay goes through a minimum vs. the electron density, the minimum always occurring at a density for which the plasmon frequency and LO phonon frequency resonate. When converted to sheet density, the resonance point could be shifted to higher sheet densities by electrically heating the electrons. Companion experiments involving FET degradation, carrier velocity as determined by the current gain cut off frequency, and change in low frequency noise were conducted. It should be noted that the low frequency noise technique is relatively much more sensitive and unique to our work. Strikingly, all the aforementioned observations are consistent in that the device degradation is minimum at the above discussed resonance, the current gain cut off frequency and thus the carrier velocity under the gate is the highest at the resonance, and the change in the low frequency noise which is sensitive to traps is minimum at the same resonance.

These investigations truly shed a new light on the topic in that LA phonon consideration is NOT the only deterministic parameter that should be relied on in the realm of heat removal from FET channels. Our study demonstrates and asserts that LO phonon decay to LA phonon is the bottleneck mechanism and that device should be operated at or near the resonance for efficient heat removal and thus reduced damage under operation. Furthermore, the same resonance also leads to the most efficient removal of LO phonons which bode well for carrier transport as confirmed by the current gain cut off frequency investigations we conducted. As will be discussed, we propose, actually commenced the preliminary investigations, a dual channel structure with camelback like electron distribution in the direction vertical to the channel to widen the range of operation with the most efficient LO phonon decay. Once the LO phonon energy is transferred to LA phonons, one can then begin considering the impact of thermal conductivity which is governed by LA phonon propagation. Our effort confirms what should be

known, but is often not, which is that insightful investigation and identification of the underlying physics invariably lead to uncovering the critical processes taking place which then pave the way for effective solutions for optimum device operation. Finally, note that much of the work reported here was conducted in collaborations with Prof. A. Matulinois and his team at the Semiconductor Physics Institute, Vilnius, Lithuania also under the sponsorship of the AFOSR through EOARD, the London office.

Background

GaN-based heterostructure field effect transistors (HFETs) are poised to dominate the high frequency-high power amplifier and switching markets.^{1,2} In fact, AlGaN-based HFET structures are already available commercially for high power, moderate frequency applications. In the quest for increased cutoff frequencies, shorter gate lengths have been employed, but two-dimensional electron gas density (2DEG density) has also been observed to play a role in cutoff frequencies among devices from the same group.^{3,4} For a given gate length, the cutoff frequencies tend to decrease with increasing 2DEG density. This can be explained in terms of the buildup of population of longitudinal optical (LO) phonons in the GaN channel.^{5,6,7} The physical origin of the buildup is related to the fact that the time associated with the emission of LO phonons by hot electrons is much shorter than the time associated with the decay of these LO phonons into acoustic phonons. Consequently, the population builds-up, causes stronger electron scattering, and results in a decrease in electron drift velocity.^{6,8} In addition to affecting the frequency performance of the HFET, the buildup is believed to be linked to the device reliability since the hot phonon population inevitably stimulates defect generation. Moreover, this can be envisaged when one considers that the hot phonons are crowded in a relatively narrow portion of the k -space where their equivalent temperature becomes extremely high.⁹ In this regard, the generation of locally large atomic vibrations and ensuing new crystal defects is likely. Correlation of the hot-phonon lifetime and device degradation has been indirectly observed.¹⁰

The time associated with the hot-phonon conversion into other vibrations (e.g. acoustic and other phonons) is referred to as the hot-phonon lifetime, and this lifetime is responsible for the hot phonon population that builds up when power is supplied to the channel. The hot-phonon lifetime is a function of electron density, electron and ambient temperatures, and other conditions. In particular, time-resolved Raman studies in bulk GaN show that the hot-phonon lifetime decreases from about 2.5ps to 0.35ps as the carrier density increases from 10^{16} to 10^{19} cm^{-3} .¹¹ The monotonous decrease of the lifetime in bulk GaN is understood in terms of coupling of LO phonons with plasmons.¹²

Estimating the average three-dimensional electron density (3D density) in an HFET channel simply by dividing the sheet density by the effective width of the triangular quantum well at the Fermi energy we see that densities of the order of 10^{19} cm^{-3} and higher are readily attainable in the GaN channel of an HFET. As such, one might expect the hot-phonon lifetimes to be less than 0.35ps in most 2DEGs. However, this often does not turn out to be the case. Experimental data on the hot-phonon lifetime in GaN 2DEGs at low applied fields obtained mainly through the microwave noise technique¹³ are illustrated in **Figure 1** (open symbols).

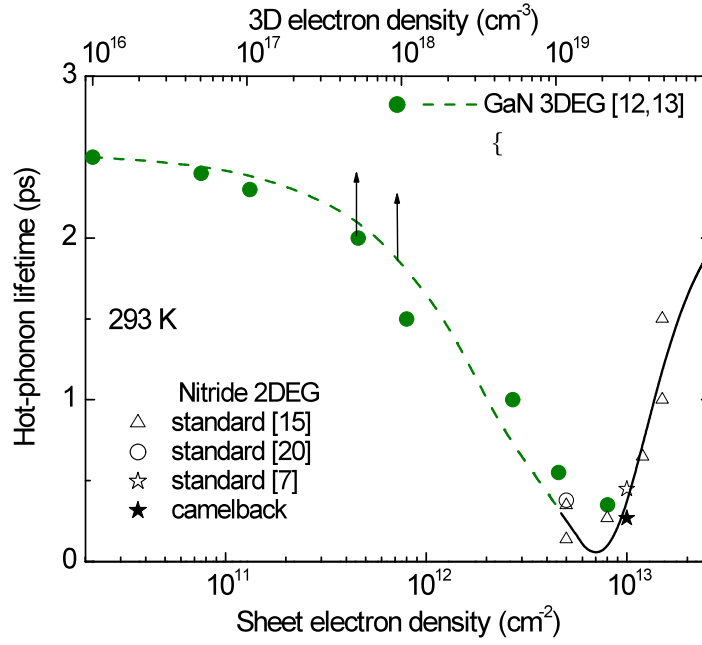


Figure 1. A survey of measured low field hot-phonon lifetimes for bulk GaN (closed circles¹¹) and various GaN-based 2DEG channels (open symbols^{7,14,15}) as well as the (Al_{0.1}Ga_{0.9}N/GaN) camelback channel (closed star) as the solution we are proposing for increasing the sheet density while remaining at the bulk resonance for minimum LO phonon lifetime. Dashed line stands for plasmon-LO-phonon model.¹² Solid line guides the eye.

In a GaN quantum well, the notion of a bulk-like plasmon mode is not unrealistic if one takes into account that the plasmon wavenumbers are of the order of the hot-phonon wavenumbers ($\sim 1 \times 10^{-9} \text{ m}^{-1}$) launched by hot electrons⁷ while the well width is several nanometers.

Regardless, for infinite electron plasma, the plasmon and phonon frequencies are equal at the electron density,

$$n_{res} = \omega_{LO}^2 \frac{m_e^* \epsilon}{e^2},$$

Equation 1

where ω_{LO} is the LO-phonon frequency and ϵ is the dielectric constant.¹⁴ This electron density, the resonance density, is estimated to be around 10^{19} cm^{-3} in bulk GaN. The coupled mode becomes important near the resonance electron density, $\sim 10^{19} \text{ cm}^{-3}$, or alternatively near $\sim 5 \times 10^{12} \text{ cm}^{-2}$ for a typical GaN 2DEG channel if the average 3D density in the channel is estimated as the 2DEG density divided by the width of the triangular well at the Fermi energy. The fastest decay of hot phonons is expected near the plasmon–LO-phonon resonance, and thus the lifetime is long at high densities where the plasmon energy exceeds the LO-phonon energy.¹⁴ Despite the simplistic nature of the model, it appears to be in reasonable agreement with the non-monotonic dependence of the hot-phonon lifetime on the 2DEG density measured at low fields for various nitride heterostructures (Figure 1, open symbols and solid line).

In light of the resonance phenomenon, the key to ultrafast decay of hot-phonons at high 2DEG densities (higher than the resonance 2DEG density estimated for standard 2DEG channels, Figure 1) is in spreading the electrons in real space so that their 3D density can be made closer to the resonance density.¹⁶ We have illustrated this concept by presenting the measured hot-phonon lifetimes for two similar samples with almost identical 2DEG densities ($1 \times 10^{13} \text{ cm}^{-2}$) when a lower average bulk electron density is achieved in a composite $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}/\text{GaN}$ channel. The composite structure exhibits a “camelback” electron density profile under electron heating. The camelback profile is expected to have a bulk electron density closer to the resonance density needed to achieve the shortest hot-phonon lifetime.

Results

Camel back structure for increased sheet density while remaining at the resonance

In order to estimate the effects of the camelback channel on the electron distribution in the 2DEG, Schrödinger–Poisson equations were solved for the structure in question as well as a standard HFET structure without the $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ interlayer. Results from the calculation are displayed in [Figure 2](#). One can observe two important points in the camelback device from [Figure 2](#); first, the conduction band edge changes from the typical quasi-triangular well shape in the vicinity where the 2DEG ultimately forms into a pair of quasi-triangular wells due to the conduction band offsets at both the $\text{AlN}/\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ and $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}/\text{GaN}$ interfaces. This phenomenon gives rise to the second and most important point: despite the same total charge in the channel ($1 \times 10^{13} \text{ cm}^{-2}$), the electrons have been effectively spread out in the camelback channel and resulted in a reduced peak 3D electron density as compared to the 2DEG in the standard structure. This is important as the 3D electron density is believed to be the parameter responsible for hot-phonon interaction with plasmons; once the 3D density is reduced, the hot-electron–hot-phonon system is closer to the plasmon–LO-phonon resonance and exhibits shorter hot-phonon lifetimes.

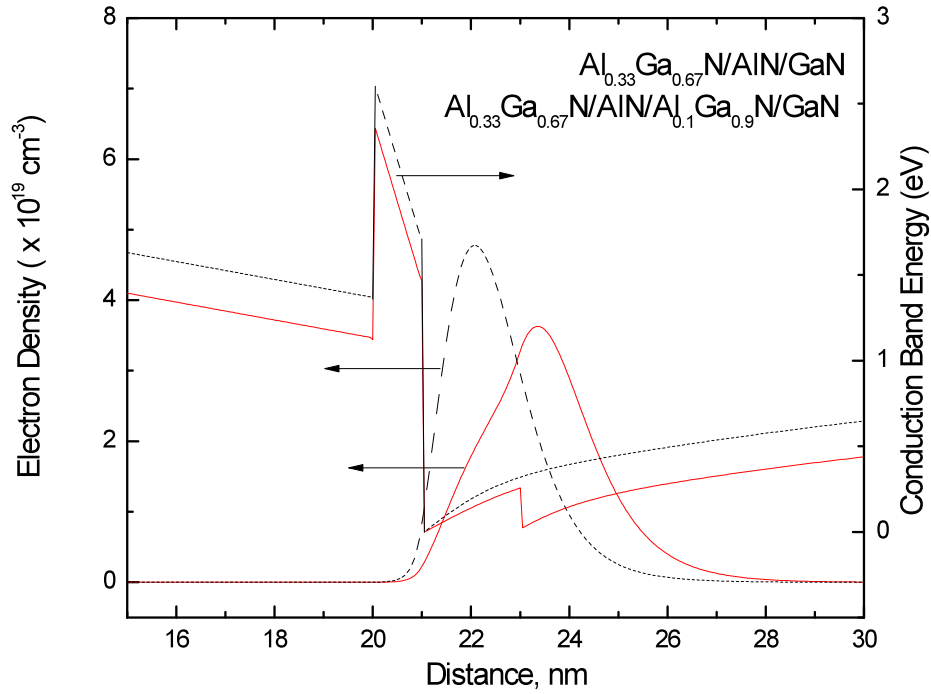


Figure 2. Calculated conduction band edge and electron 3D density for a standard (dashed lines) as well as the $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ camelback channel structure (solid lines). The total numbers of electrons are equal ($1 \times 10^{13} \text{ cm}^{-2}$) in each channel.

In light of the fact that hot electrons within a GaN-based HFET channel are known to reach 1000's of K under bias, Schrödinger–Poisson equations have been again solved at elevated electron temperatures for the camelback structure. The results are displayed in Figure 3. One can see the expected spreading of the electron distribution with the temperature, resulting from the increased occupation of upper subbands by hot electrons in the coupled wells of the composite channel. Due to this, the camelback shape of the profile for which the structure is named begins to emerge; it appears as though the original 2DEG is splitting, with the resultant 2DEG having lower overall 3D density but in fact containing the same total charge ($1 \times 10^{13} \text{ cm}^{-2}$).

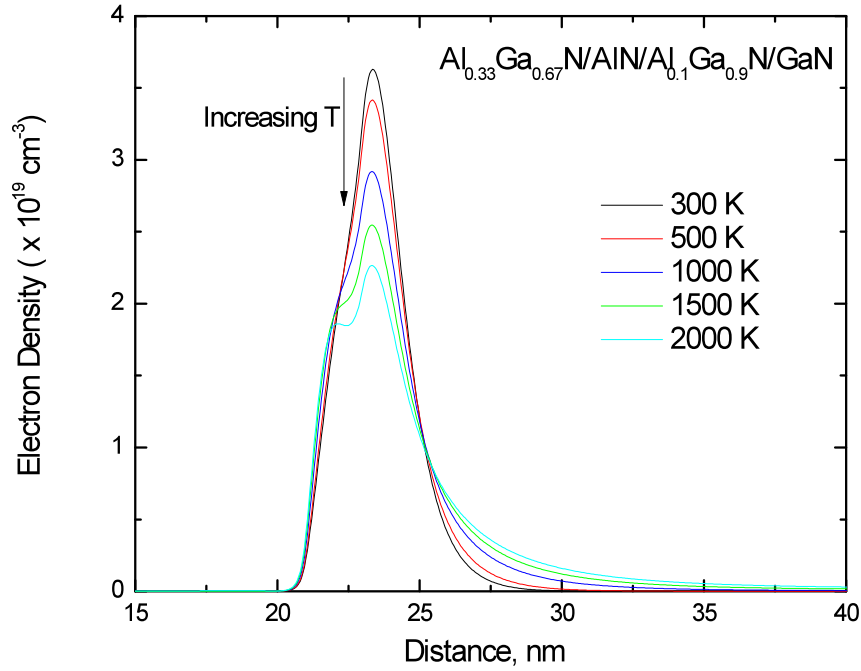


Figure 3. Calculated electron 3D density as a function of electron temperature for the camelback structure. In each curve, the integrated density of electrons equals $1 \times 10^{13} \text{ cm}^{-2}$. The dual peaked 2DEG (camelback) is pronounced at elevated temperatures.

From the simulations, it is apparent that the camelback approach is effective in reducing the peak 3D density of a 2DEG with a fixed total charge ($1 \times 10^{13} \text{ cm}^{-2}$ in this case). To access this information experimentally, capacitance–voltage (C–V) measurements can be employed to plot electron 3D density profiles as a function of the depth into the structure. Subsequently, the total 2DEG density can be estimated by integrating these 3D densities obtained from the C–V measurement. Shown in [Figure 4](#) are the experimental density profiles for the camelback structure as well as a standard AlGa_N/AlN/GaN structure⁷ for comparison. The standard structure was selected due to its similarity to the camelback structure in terms of the total 2DEG density; through integration, the standard and camelback structures exhibit total 2DEG densities

of 0.99×10^{13} and $1.02 \times 10^{13} \text{ cm}^{-2}$, respectively. Despite the similarity in 2DEG densities, the half-width of the 2DEG in the camelback structure ($\sim 0.8\text{nm}$) is larger than that of the standard structure ($\sim 0.6\text{nm}$), as anticipated from the simulation. Thus, the camelback structure with a lower 3D electron density than the standard structure should exhibit a shorter hot-phonon lifetime than the standard structure.

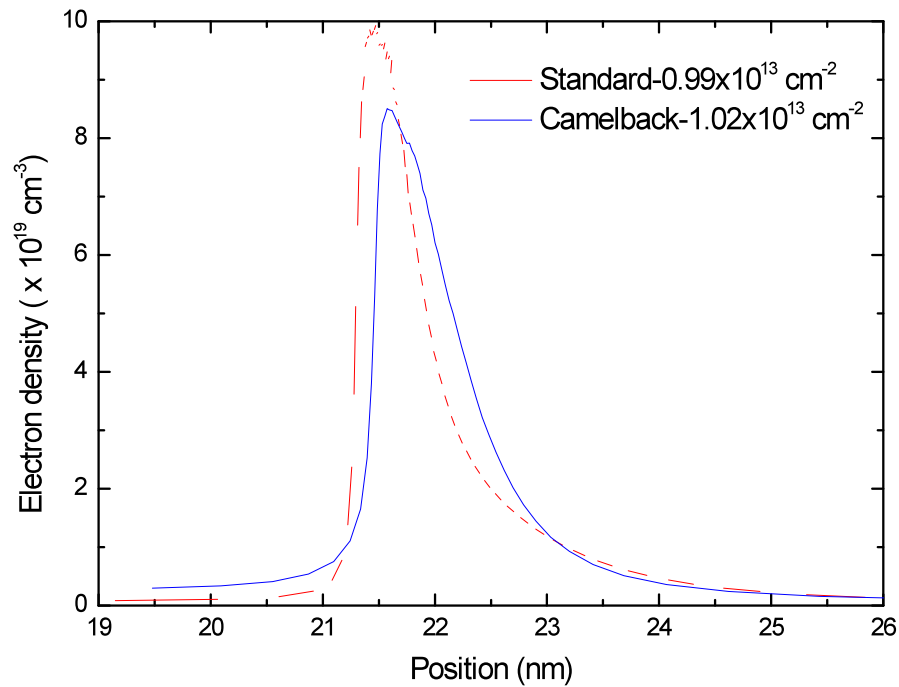


Figure 4. Electron 3D density profiles measured by capacitance–voltage technique for the camelback structure (solid) as well as the standard structure (dashed).

To obtain the hot-phonon lifetime in a 2DEG, the microwave noise technique is employed.¹³ In this technique, voltage pulses are applied to a pair of Ohmic contacts, and the noise power emitted from the channel at 10GHz is compared to that of a blackbody radiator kept at a known temperature. Since the sample is not a true blackbody, additional measurements are performed for estimation of the sample reflection coefficient at each bias and power loss in the input

microwave circuit. At 10GHz, low frequency sources of noise such as 1/f noise and noise associated with trapping can be neglected—the microwave noise can be attributed to electron scattering.

Figure 5 shows the measured excess noise temperature (temperature in excess of room temperature) as a function of the power supplied to an average electron present in the camelback channel. The circles represent the temperature estimated for voltage pulse duration of 2.7 μ s while the squares and triangles stand for 100ns and 50ns pulse durations, respectively. The equivalent results for both pulse widths at moderate pulsed power in the camelback structure indicate no self-heating.

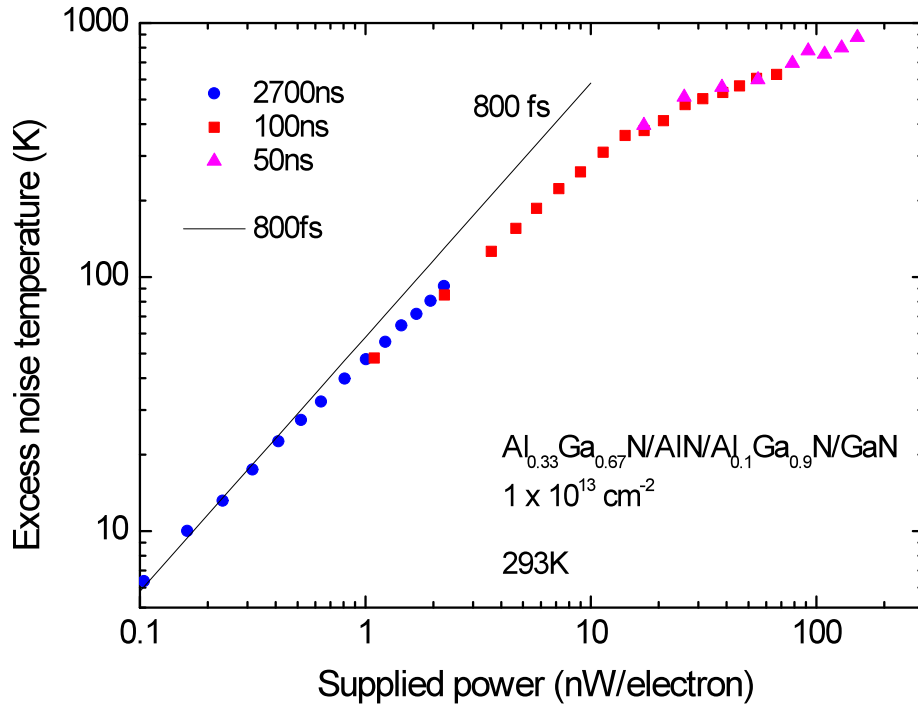


Figure 5. Measured excess noise temperature, equal to the electron temperature, for the camelback structure as a function of applied power. Circles represent pulse widths of 2.7 μ s, squares stand for 100ns, and triangles represent 50ns.

Let us now consider the power dissipated by hot phonons. Once a constant hot-phonon lifetime ω_{LO} is assumed, the dissipated power is proportional to the excess occupancy of the hot phonon modes, $P_d = A(N_{LO}^* - N_0)$ where N_{LO}^* is the equivalent occupancy of the LO-phonon states (occupied by the hot phonons emitted by the hot electrons) and $A = \hbar\omega_{LO}/\tau_{LO}$. For the dominant electron–LO-phonon interaction and strong hot-phonon effects, the noise temperature, T_{noise} , approximately equals the hot-electron temperature, T_e , while the latter almost equals the equivalent hot-phonon temperature T_{LO} .¹⁷ Thus, the equivalent occupancy N_{LO}^* can be estimated after the Bose–Einstein formula if $T_{LO}^* \approx T_e$ is assumed (the validity of the assumption has been checked previously^{17,18,19}). This leads to:

$$P_d = A \left\{ \left[\exp\left(\frac{\hbar\omega_{LO}}{k_B T_e}\right) - 1 \right]^{-1} - \left[\exp\left(\frac{\hbar\omega_{LO}}{k_B T_0}\right) - 1 \right]^{-1} \right\}$$

Equation 2

Equation 2 is a modified Arrhenius law. It states that an electron can take part in power dissipation if its energy exceeds the LO phonon energy. Solid lines in Figure 6 illustrate Equation 2 when constant values of 200 and 300 fs are used for the hot-phonon lifetime. Note that the experimental data (symbols) remain in between the curves in the temperature range below ~ 600 K ($\sim 1.6 \cdot 10^{-3}$ K⁻¹). In this range, the power dissipation is mainly controlled by the electron interaction with the hot LO phonons treated in terms of constant hot-phonon lifetime.

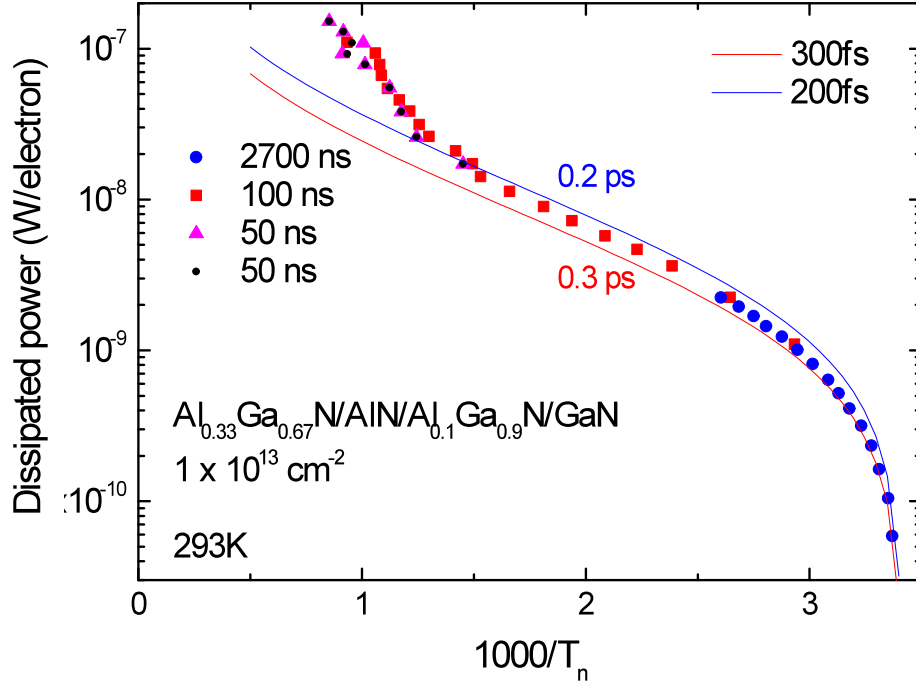


Figure 6. Arrhenius plot of experimental dissipated power against inverted noise temperature for the camelback structure (symbols) along with Equation 2 that assumes constant hot-phonon lifetimes of 200fs and 300fs (solid lines, blue and red, respectively).

However, the hot-phonon lifetime seems to depend on the applied power at high temperatures, and a dynamic lifetime can be introduced:

$$\tau_{LO}^* = \hbar \omega_{LO} dN_{LO}^* / dP_d$$

Equation 3

Figure 7 shows the results for the dynamic hot-phonon lifetime as a function of the supplied power for the camelback structure (squares). At low-moderate supplied pulsed powers (<10nW/e), the hot-phonon lifetime for the camelback channel structure is nearly constant and approximately equals ~270fs.

Electron energy dissipation is often treated in terms of hot-electron energy relaxation time. Under a fixed value of the relaxation time, τ_{energy} , the electron temperature increases linearly with applied power, P_A , in accordance with $k_B(T_e - T_0) = P_A \tau_{energy}$. The energy relaxation time at zero applied power is close to 800fs (solid line in Figure 5). This value exceeds the low-power value of the hot-phonon lifetime of 270 fs estimated in the power range below 10 nW/electron where the lifetime is almost independent of the power (Figure 7, squares). The energy relaxation time appears to depend on the applied power as well. In this case, a dynamic energy relaxation time can be introduced, $\tau_{energy}^* = k_B dT_e / dP_A$, which is plotted in Figure 7 (circles). The value of the energy relaxation time appears to be ~700–800fs under low (<1nW/electron) supplied power, but decreases with increasing supplied power, and eventually τ_{energy}^* merges with the dynamic hot-phonon relaxation time τ_{LO}^* at a power of ~10 nW/electron. This happens at a hot-electron temperature exceeding ~600K (Figure 5) when many of the electrons have sufficient energy to emit LO phonons.

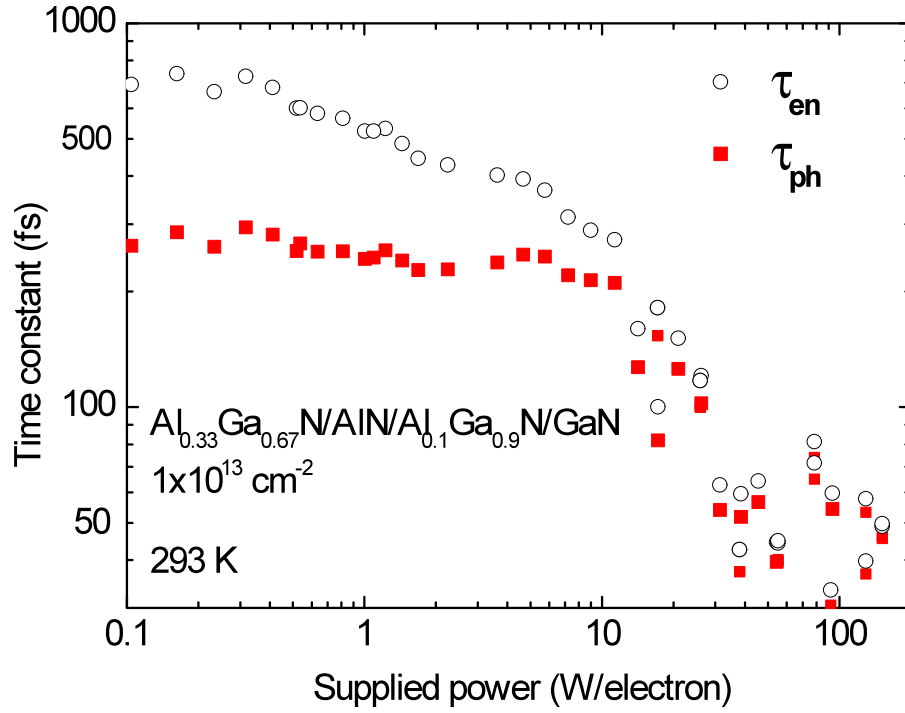


Figure 7. Dynamic energy relaxation time (circles) and dynamic hot-phonon lifetime (squares) as functions of the supplied power for the camelback structure.

Figure 8 compares the hot-phonon lifetime for two camelback channels (triangles and stars) and a reference channel (squares) when the channels have the same 2DEG density ($1 \times 10^{13} \text{ cm}^{-2}$). Two important phenomena are noted. First, the low-power value of the hot-phonon lifetime is reduced from $\sim 500 \text{ fs}$ in the standard channel to $\sim 270 \text{ fs}$ in the camelback channel. Next, both the camelback channel as well as the standard channel exhibit a rapid decline in the hot-phonon lifetime at high power levels, but several times higher power is needed for the decline to take place in the standard channel. The properties of the camelback channel are reproducible (stars and triangles).

Let us compare further the results for the camelback channel and the standard one (Figure 8). Despite nearly identical 2DEG density ($1 \times 10^{13} \text{ cm}^{-2}$), the channels have different electron density profiles (Figure 4). The electron 3D density is lower in the camelback channel, and the plasma frequency is closer to that of the LO phonons. In accordance with the plasmon-assisted decay of hot phonons, the camelback channel demonstrates the reduced hot-phonon lifetime at low power, Figure 8 (stars, triangles). Under electron heating, the power-assisted spreading of the electron density profile takes place and causes the 3D density to approach the plasmon–LO-phonon resonance value.¹⁴ This happens in both the camelback channel as well as the standard structure, and the associated rapid decline in hot-phonon lifetime is observed at elevated power levels. However, the camelback structure exhibits the rapid decline in hot-phonon lifetime at a lower supplied power than the standard structure, despite having equal total 2DEG densities.

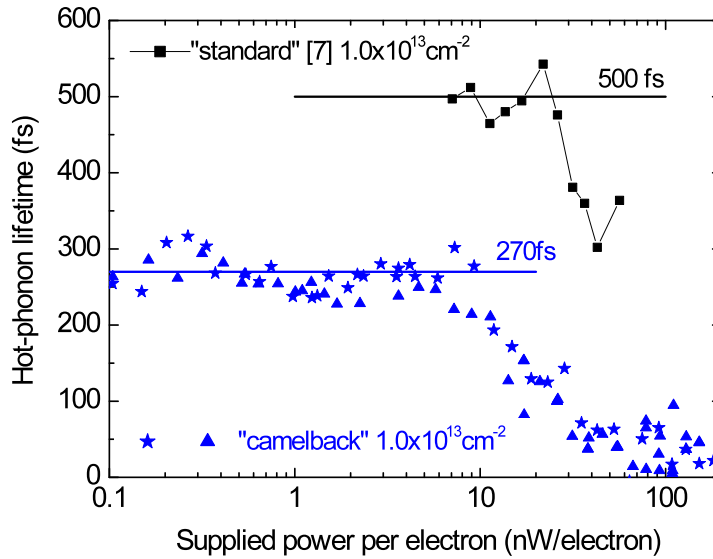


Figure 8. Hot-phonon lifetime measured by the microwave noise technique for the standard channel (squares) as well as camelback channels (stars, triangles) with equal 2DEG densities ($1 \times 10^{13} \text{ cm}^{-2}$).

The decline in hot-phonon lifetime with supplied power is attributed to a significant spreading of the electron density profile when the electrons begin to fill the second subband of the quantum well at the hot-electron temperatures associated with these supplied powers (above 600K according to [Figure 5](#) and [Figure 6](#)). Such a phenomenon is evidenced from the simulation in [Figure 3](#) which shows the electron profile as a function of the electron temperature. Significant profile spreading takes place between temperatures from 500K to 1000K according to [Figure 3](#). Higher electron temperatures and consequently higher applied power are required to fill the upper sub-bands in the standard structure,¹⁴ and therefore the rapid decline of the hot-phonon lifetime is not achieved until several times higher power is applied to the standard structure. The camelback structure has been successfully designed to reduce the 3D density of electrons in an HFET channel at zero bias and demonstrates a shorter low-power value of the hot-phonon lifetime at a given 2DEG density. Moreover, it also exhibits a lower threshold for the rapid decline of the hot-phonon lifetime caused by the power-assisted spreading of the 2DEG profile.

As can be gleaned from the above discussion the dual channel device, with camelback like electron profile in the vertical direction, holds a good deal of promise in that it allows one to increase the total electron concentration while staying at or near the plasmon-LO phonon resonance, and thus further elaboration of this structure is warranted. We have taken the first set of steps for a comparative analysis of camelback FETs vis. a vis. conventional structure which also included simulations of the carrier distribution and extraction of FET parameters. What we can say at this point of progression is that the maximum carrier velocity, as deduced from RF

transit time measurements, for the camelback structure takes place at twice the 2DEG density of that of the conventional. However, the carrier densities for both structures at which the velocity is maximum is about half of that which corresponds to the plasmon LO phonon resonance. We would like to remind the reader that there are preliminary data and additional experiments would need to be conducted which we are in the process of doing. Below, we systematically discuss the conventional and camelback HFET data, albeit preliminary.

The simulation of the vertical electron distribution is first discussed in the context of InAlN barriers, which is not exceedingly critical, as AlGa_N barriers could have been equally chosen, with various thicknesses of AlGa_N channel augmenting the juxtaposed GaN channel. One benefit is that relatively large carrier concentrations, beyond the resonance point, can be attained.

The structure is shown in [Figure 9](#), compared with the conventional InAlN/GaN HFET structure. Silvaco ATLAS is used to optimize and simulate the Al composition and thickness of AlGa_N channel. As discussed earlier, the basic idea for the optimization is to reduce the peak electron concentration in 2DEG channel and spread out the electrons in a wider channel. At first we tried to tune the Al composition of AlGa_N channel. The 2nm AlGa_N channel layer with Al composition of 10%, 17% or 20% was inserted into the conventional HFET structure.

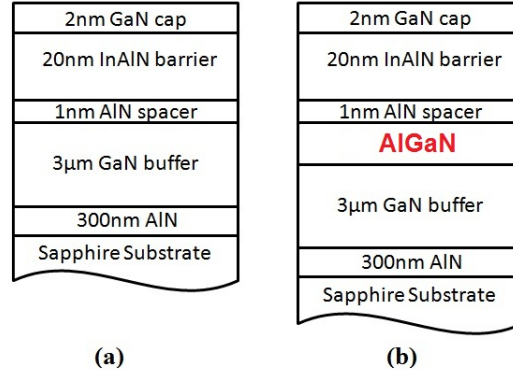


Figure 9. The diagram of conventional InAlN/AlN/GaN (a) and the novel InAlN/AlN/AlGaN/GaN camelback structure to be optimized (b).

Guided by the simulation it is found that the 10% AlGa_N channel augmentation layer is the best option to reduce the peak electron concentration by spreading the carriers. Arguably this will lead to a larger variation of the transconductance with gate bias as compared to the single channel ones, within the limitation of the particular design considered here. However, this should be weighed along with the benefits that are being discussed here. As shown in **Figure 10**, with the Al composition decreased, the peak electron concentration in 2DEG channel is reduced. The AlGa_N augmented channel with 10% Al was chosen for experimental investigation at the initial stages. The 5% sample has recently been prepared and is in the process of fabrication and evaluation.

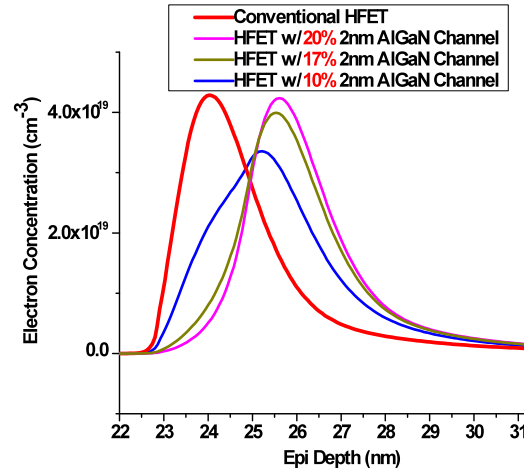


Figure 10. The electron concentration profiles for InAlN/AlN/AlGaN/GaN HFET structure with a 2nm AlGaN channel augmentation in addition to the GaN channel, with 10%, 17% and 20% Al mole fraction.

Secondly the AlGaN channel thickness is optimized as well. As shown in [Figure 11](#) and [Figure 12](#), the AlGaN channel with thickness of 2, 3, and 4nm is employed to the HFET structure. The Al composition of AlGaN channel is 10%, as optimized and mentioned above. It can be seen that, with the AlGaN channel thickness increased, the peak electron concentration is reduced more.

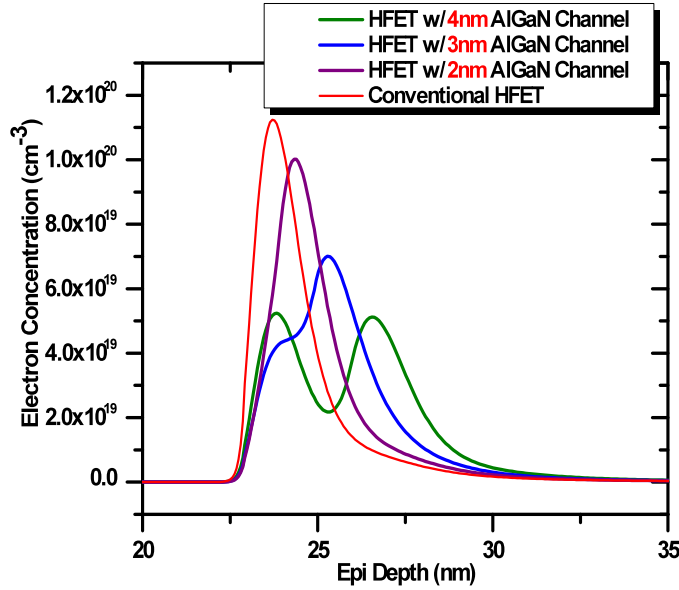


Figure 11. The electron concentration profiles for the HFET structure with 2, 3 and 4nm $\text{Al}_{0.1}\text{Ga}_{0.9}\text{N}$ channel.

It is also noted that when the AlGaIn channel thickness is increased to 4nm the electron distribution manifests itself as two separate peaks, [Figure 11](#). We also note that for the 4nm AlGaIn channel, the electrons distribute in AlGaIn channel and GaN channel nearly evenly. Note that these are low energy electrons in equilibrium with the lattice. Once under the influence of large lateral field, they gain energy and become hot in which case the distribution would vary. As well known, alloy scattering is introduced to the 2DEG channel by the AlGaIn channel. If electrons distributed in AlGaIn channel is equal to or more than those in GaN channel, more than half of electrons would suffer alloy scattering, which would degrade the low field mobility in 2DEG channel. However, the low field mobility affects the access resistances and also the resistance of the portion of the channel under the gate not experiencing high fields. In the high field region, the dispersion between the electron mobilities in GaN and low mole fraction AlGaIn, which is under discussion here, should be negligible. Using the low field mobility concern, we consider the 3nm thickness for the AlGaIn channel to be a good choice. As shown in

Figure 11, with 3nm AlGa_{0.1}N channel, the peak electron concentration is still significantly reduced.

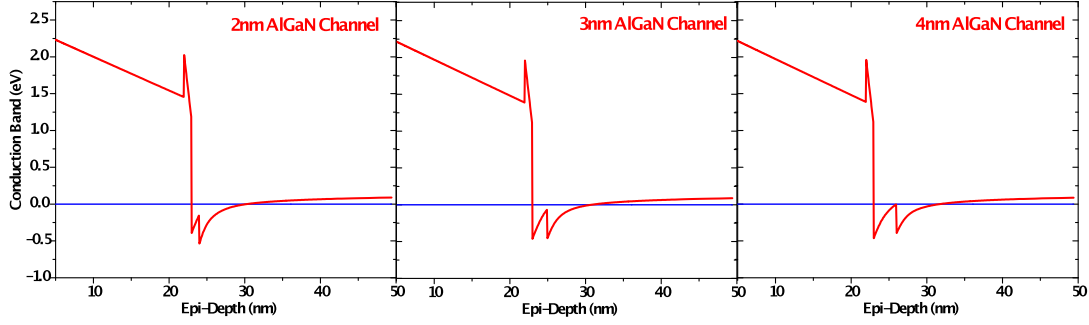


Figure 12. The conduction band diagrams for the HFET structure with, from left to right, 2, 3 and 4nm Al_{0.1}Ga_{0.9}N channel.

From the simulation and optimization mentioned above, it can be concluded that, the optimum thickness and Al composition for the AlGa_{0.1}N channel augmentation layer are 3nm and 10%, respectively. In concert with this rationale, we proceeded with the aforementioned AlGa_{0.1}N channel HFET parameters for the HFET portion of this investigation, as follows:

An AlGa_{0.1}N/GaN dual channel HFET structure with AlInN barrier and a control InAlN/AlN/GaN HFET structure were grown on 2 inch (001) sapphire substrates with low-pressure custom-designed organometallic vapor phase epitaxy (OMVPE). Standard fabrication methods were applied to produce approximately 1 micron gate devices. Electrical measurements, inclusive of DC and low signal RF using a network analyzer, were conducted. The equivalent circuit

parameters with both gate bias and drain bias, and therefore drain current, as variable parameters were extracted. Also extracted were the charging transit time associated constants in order to determine the intrinsic transit time and thus the electron velocity in high fields.

The DC output characteristics of InAlN barrier control HFETs as well as the InAlN barrier and AlGaIn/GaN dual channel HFETs as shown in **Figure 13**.

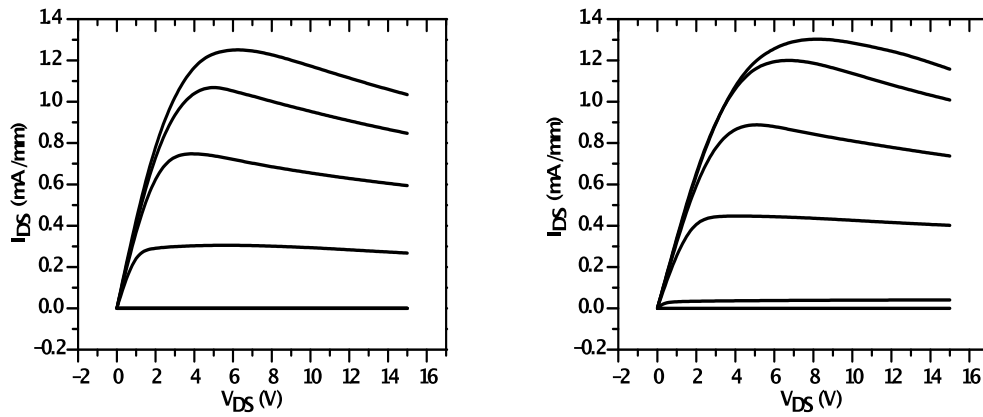


Figure 13. I-V characteristics of (a) InAlN control HFET and (b) AlGaIn/GaN dual channel HFET on sapphire substrate. The gate voltage was varied from 0 V to -8 V with 2V steps for (a) and from 0V to -10 V with 2 V steps for (b). The pinch-off voltage is -8V and -9V for the AlGaIn/GaN dual channel and control HFETs, respectively.

All the HFETs under discussion have a 1.1 μ m gate length with 90 μ m gate width and 4 μ m source-drain separation. It can be noted that the saturation current density (1.35A/mm) for the AlGaIn/GaN dual channel HFET is comparable with the control HFET sample (1.29A/mm).

In order to determine the electron distribution, vertically, which goes to the heart of the issue, we conducted Capacitance-voltage (C-V) measurements. The electron concentration for both the control sample and the camelback structure as a function of depth is plotted in Figure 14. Note that the electron concentration peak is shifted farther into the GaN buffer layer for the AlGaIn/GaN dual channel (camelback) HFET because of the introduction of the extra AlGaIn channel layer. The peak concentration of the AlGaIn/GaN dual channel HFET is $1.0 \times 10^{20} \text{ cm}^{-3}$, substantially lower than that for the control HFET which is $1.9 \times 10^{20} \text{ cm}^{-3}$. By integrating the curves, the 2DEG densities for the AlGaIn dual channel and control HFETs were found as $2.0 \times 10^{13} \text{ cm}^{-2}$ and $1.7 \times 10^{13} \text{ cm}^{-2}$, respectively. The point is that the total 2DEG density of the AlGaIn/GaN dual channel HFET is higher than that of the control HFET and the associated electron concentration profile is wider with desired effect of lower peak concentration.

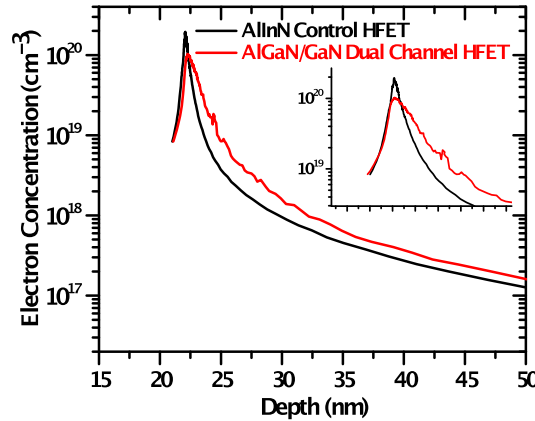


Figure 14. Electron concentration versus depth profile calculated from the C-V data, measured from the Schottky diodes next to the HFET patterns. The red and black curves represent the AlGaIn/GaN dual channel and control HFETs respectively. In the inserted figure, the peak region is shown and the depth is normalized for a clear comparison.

On-wafer microwave measurements were carried out using a HP1850B vector network analyzer over a range of 2 to 20GHz. The S-parameters were collected to calculate the small signal current gain, h_{21} and cut-off frequency under different DC bias conditions. The maximum cut-off frequency for the AlGaIn/GaN dual channel HFET is 14.7GHz, associated with the bias condition of $V_{DS} = 4V$ and $V_{GS} = -6V$. In comparison, the control HFET exhibited a cut off frequency of 15.4GHz, comparable, under the bias conditions of $V_{DS} = 4V$ and $V_{GS} = -5.5V$, as shown in Figure 15. The comparable cut-off frequencies indicate that the performance of AlGaIn/GaN dual channel HFET was not degraded by the extra AlGaIn layer in the structure.

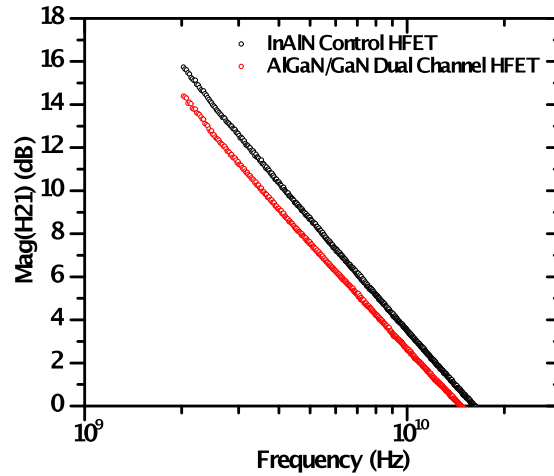


Figure 15. Unity current gain for the AlGaIn/GaN dual channel (red) and control (black) HFETs. The cut-off frequency is $f_T = 14.7\text{GHz}$ at bias of $V_D = 4V$ and $V_G = -6V$ for the AlGaIn/GaN dual channel HFET and $f_T = 15.4\text{GHz}$ at bias of $V_D = 4V$ and $V_G = -5.5V$ for the control HFET.

Following the approach reported by Moll *et. al.* [20], we delineated the intrinsic transit time for these two samples which allowed the determination of the saturation velocity at the different bias

conditions. Firstly the total delay times ($\tau_{\text{total}}=1/(2\pi f_T)$) at a constant gate bias with varied drain bias were determined and plotted versus the voltage drop across the channel, as shown in **Figure 16 (a) and (c)**. Following the method presented in Ref [21], we obtained R_S+R_D values of 15 and 21Ω for the AlGaIn/GaN dual channel HFET and control HFET, respectively. By fitting the linear parts of the curves and extrapolating to the vertical axis where the channel voltage equals zero, we determined the intrinsic transit time delay plus the channel charging time of HFETs ($\tau_{\text{int}}+\tau_{\text{RC}}$). This approach allows us to isolate out the drain delay. Secondly by plotting the total delay times, measured at a constant drain bias but with varied gate bias, vs. the inverse drain current, the intrinsic transit time plus the drain delay ($\tau_{\text{int}}+\tau_{\text{D}}$) can be determined, as shown in **Figure 16 (b) and (d)**. After the $\tau_{\text{int}}+\tau_{\text{RC}}$ and $\tau_{\text{int}}+\tau_{\text{D}}$ values are determined, the intrinsic transit time at different bias can be calculated. It should be reminded that the data analyses in general and extrapolations in particular are preliminary in nature, which require further investigations to be certain about the exact figures, a process which is in progress.

As expected the minimum intrinsic times appear at the bias points with the highest cut-off frequencies. For the AlGaIn/GaN dual channel HFET, the intrinsic time is 8.8 ps at the bias condition of $V_{\text{DS}} = 4\text{V}$ and $V_{\text{GS}} = -6\text{V}$. For the control HFET, the intrinsic time is 8.6ps at the bias condition of $V_{\text{DS}} = 4\text{V}$ and $V_{\text{GS}} = -5.5\text{V}$. Using $v = L_G/\tau_{\text{int}}$ (L_G is the gate length of the HFETs), the average electron velocities for the AlGaIn/GaN dual channel HFET and the control HFET were determined as $1.28 \times 10^7 \text{cm/sec}$ and $1.25 \times 10^7 \text{cm/sec}$, respectively, which are very similar as expected. This is due to the fact that electron velocity at high fields in both GaN and low fraction AlGaIn are comparable even though the low field mobilities are different because of addition of alloy scattering in the latter.

By integrating the electron concentration *vs.* depth with respect to the applied voltage, the 2DEG densities corresponding to the particular bias points mentioned above can be determined as $3.7 \times 10^{12} \text{cm}^{-2}$ and $6.1 \times 10^{12} \text{cm}^{-2}$ for control HFET and the dual channel AlGaIn/GaN HFET, respectively. These carrier densities are approximately half of what is expected from the consideration of plasmon LO phonon resonance which causes the LO phonon lifetime to be the minimum. We are in the process of conducting more precise experiments paying specific attention to details, particularly the quality of samples as judged from low field mobility, etc. The low field electron mobility in the dual channel device measured is as low as $200 \text{ cm}^2/\text{Vs}$ which is too low. The current samples that are in the process in the laboratory exhibit nearly $1000 \text{ cm}^2/\text{Vs}$ electron mobilities. We expect to finish fabrication and data analyses soon and revisit the issue of carrier density at which the minimum transit time is achieved.

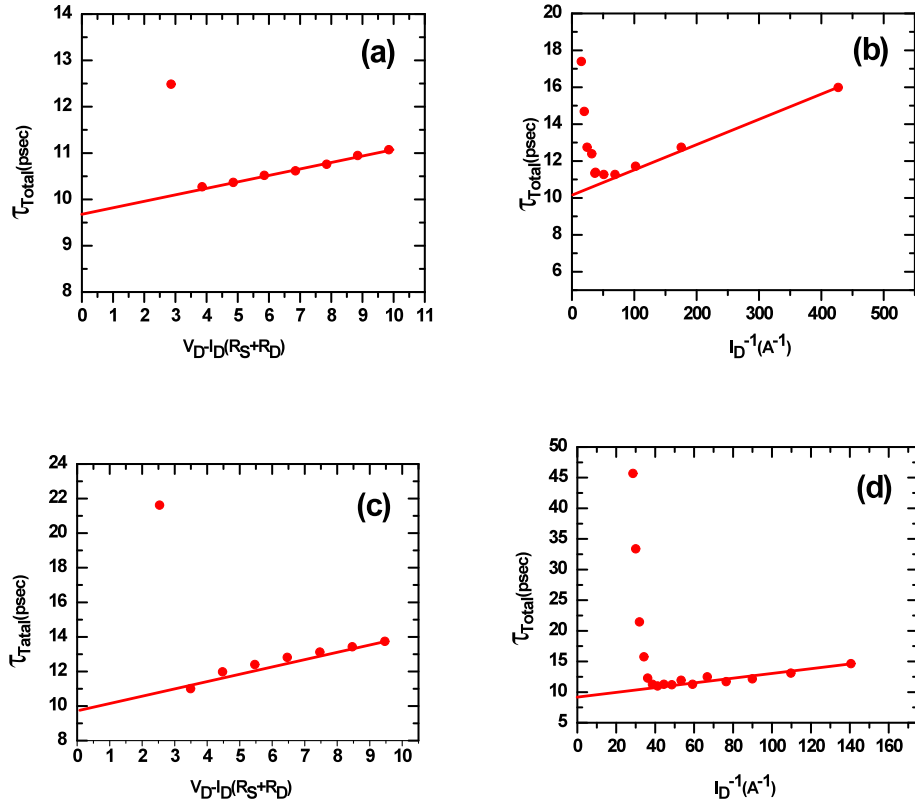


Figure 16. Total delay time versus channel voltage to extract the total time excluding drain delay (a) for InAlN control HFET and (c) for AlGaIn/GaN dual channel HFET. Total delay time versus inverse current to extract the total time excluding parasitic RC delay (b) for InAlN control HFET and (d) for AlGaIn/GaN dual channel HFET. The solid lines are the extrapolations to zero channel voltage (a) (c) and infinite drain current (b) (d).

If we were to increase the sheet electron density in the conventional InAlN/AlN/GaN 2DEG channel, the hot phonon life time would increase and the electron velocity would decrease. However, with the extra AlGaIn channel in the HFET, in addition to the GaN one, the electrons spread out and thus the peak electron concentration is reduced, as indicated in [Figure 14](#). Even though the total 2DEG density for the AlGaIn/GaN dual channel HFET is comparable to the control HFET, more electrons operate at optimal electron concentration regime. As seen from the

results summarized in Table 1, the AlGaIn/GaN dual channel HFET operates at much higher 2DEG density than the control HFET without the electron velocity degradation.

	HFET Control	AlGaIn/GaN Dual Channel HFET
V _{gs} (V)	-5.5	-6.0
V _{ds} (V)	4	4
Intrinsic Time (psec)	8.6	8.8
Velocity (cm/sec)	1.28×10^7	1.25×10^7
2DEG Density (cm ⁻²)	3.7×10^{12}	6.1×10^{12}

Table 1. Intrinsic time, electron velocity, 2DEG density, bias conditions for AlGaIn/GaN dual channel HFET and control HFET. Note the comparable electron velocities which are expected, if one considers the high field transport which is what is in effect here. However, the sheet densities for the minimum transit time or the maximum velocities, tabulated above, are about half of that corresponding to the plasmon- LO phonon resonance. This discrepancy is now under investigation with higher quality samples having been prepared already.

To investigate the characteristics of AlGaIn/GaN dual channel HFETs in detail, the small signal extraction procedure was employed for AlGaIn/GaN dual channel HFETs and InAlN control HFETs. The equivalent circuit for the parameter extraction is shown in Figure 17.

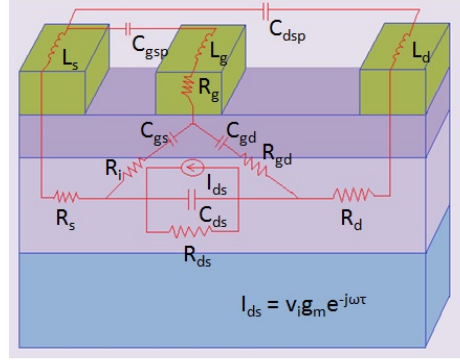


Figure 17. The equivalent circuit for small signal extraction

The “Cold-FET” method is used for the small signal extraction. At first, the pad capacitances can be extracted under the pinched-off condition ($V_{DS} = 0$, $V_{GS} \ll 0$) at low frequencies (in the megahertz range) so that the influence of inductances can be minimized. The parasitic inductance and resistance was extracted following the method reported by Chen *et. al.* [22]. Then the intrinsic components were calculated. At last, all the extracted parameters were incorporated and optimized by using Agilent ADS.

The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} for AlGaIn/GaN dual channel HFET and InAlN control HFET are plotted in Figure 18 vs. V_{gs} . It can be seen that the variation of C_{gd} for AlGaIn/GaN dual channel HFET is much larger than that for InAlN control HFET. As shown in Figure 14, with the extra AlGaIn channel in the AlGaIn/GaN dual channel HFET, the 2DEG channel becomes wider. Therefore, with the same V_{gs} applied on the channel, the depletion region variation for AlGaIn/GaN dual channel HFET is larger than that for InAlN control HFET.

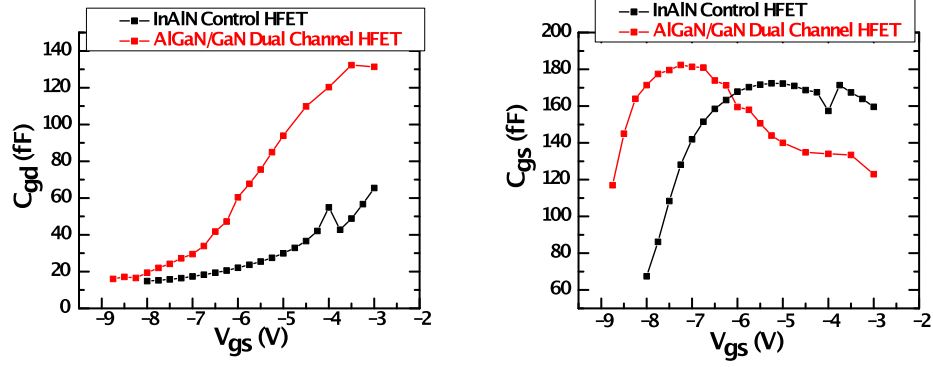


Figure 18. The extracted gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}

The intrinsic transconductance and cut-off frequency w.r.t. the gate bias are extracted and compared as well, [Figure 19](#). It can be seen that the intrinsic transconductance of AlGaIn/GaN dual channel HFET shows larger gate voltage swing (GVS) and indicates better linearity.

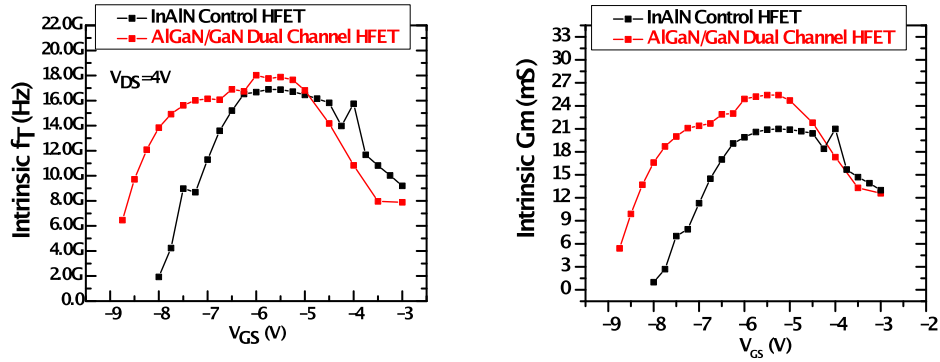


Figure 19. The extracted intrinsic cut-off frequency and intrinsic transconductance for both control and dual channel FETs.

The last parameter should be mentioned is the output resistance, R_{ds} . For power amplifiers, the output resistance is a critical parameter for output power performance. With the higher output resistance, the output power of the HFETs can be higher. As shown in Figure 20, the output resistance of AlGaIn/GaN dual channel HFET is slightly lower than that for InAlN control HFET. Typically the output resistance is related with the buffer conductivity and electron confinement of the 2DEG channel. The AlGaIn/GaN dual channel HFET spreads out the electrons in a wider channel. In the meantime, the electron confinement of the 2DEG channel is slightly degraded.-

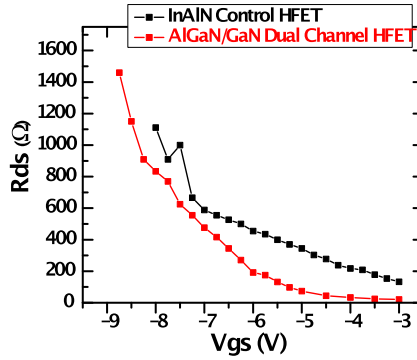


Figure 20. The extracted output resistance for both control and dual channel HFETs.

To conclude the experimental investigation of HFETs section, we introduced the novel AlGaIn/GaN dual channel HFET structure and explored its advantages over the conventional HFET structure. With the extra AlGaIn channel inserted between AlN spacer and GaN buffer, the electrons spread out and the peak electron concentration is lowered compared to the conventional GaN 2DEG channel, which is confirmed by the C-V measurement. The cut-off frequency of AlGaIn/GaN dual channel HFET is comparable to that for the InAlN control HFET. By using

Moll's method, the electron velocity below the gate is measured. It is shown that the AlGaIn/GaN dual channel HFET and the control HFET exhibit nearly the same electron velocity. However, the sheet density corresponding to the maximum electron velocity for AlGaIn/GaN dual channel HFET is almost two times higher than that for InAlN control HFET. Yet, the carrier densities at which the minimum transit time or the maximum average electron velocity occur are about half of that which corresponds to the plasmon- LO phonon resonance. This is contrary to what we expect a priori and further experiments with new and much improved heterostructures, in terms of low field mobility, are underway. We already produced the layers with low field mobility comparable to expectations and device fabrication, testing and analyses will soon begin. With small signal extraction, we compared the parasitic parameters of the AlGaIn/GaN dual channel HFET with the InAlN control HFET. The AlGaIn/GaN dual channel HFET shows better linearity. However, since the electrons are spread out by the wider channel, the electron confinement of the 2DEG channel is degraded slightly, which might be the cause for the lower output resistance than the InAlN control HFET. We should point out that these results are very preliminary in nature and we will reserve judgment until after the newly grown and much higher quality samples have gone through the process and evaluation.

Degradation in HFETs monitored by low-frequency noise: Hot phonon effects

Proverbially, higher electron concentrations lead better power performance in FETs. At first sight, InAlN/GaN-based HFET structures which reached two-dimensional electron gas (2DEG) densities up to $3 \times 10^{13} \text{ cm}^{-2}$ [23,24,25] would be highly coveted. However, this density is well above

the resonant density for the most efficient decay of LO phonons to LA phonons, see below. To reiterate, the main avenue for heat dissipation includes emission of longitudinal optical (LO) phonons by hot electrons, decay of the LO phonons into longitudinal acoustic (LA) phonons and diffusion of the excess LA phonons into the remote heat sink [26,27]. Since the LO-phonon emission by hot electrons is faster than the decay rate of these phonons to acoustic phonons, the population of the non-equilibrium LO phonons build up (referred to as hot phonons) [28]. Strong electron phonon coupling leads to hot electron and LO phonon temperature to be nearly the same [7]. The bottleneck is often quantified in terms of hot-phonon lifetime. The concept of this power dissipation bottleneck, which was described in detailed above, is crucially important for power HFET operation [29]. As noted in **Figure 1** for GaN: a minimum in the hot-phonon lifetime is found to a resonant 2DEG density of $\sim 6.5 \times 10^{12} \text{ cm}^{-2}$ at low fields [26]. The resonant 2DEG density increased with applied electric field when the resonance was resolved from the highest electron drift velocity measured for gateless GaN-based channels [30].

To underscore the deleterious effect of hot phonons, in addition to being scatterers, build-up of hot phonons at high fields increases lattice vibrations and may possibly contribute to device degradation through additional defect generation due to the already defective GaN, aided by its pyroelectric and piezoelectric crystal structure [6,31]. Likelihood of defect generation by enhanced lattice vibrations can be further supported by strong confinement of the hot phonons to a relatively narrow portion of the momentum and real spaces in an HFET channel. It then follows that the effect of hot phonons on defect generation can be minimized at the resonant 2DEG density which causes a rapid decay of hot-phonons. This has motivated the attempts to analyze degradation of performance of lattice-matched InAlN/AlN/GaN HFETs caused by electrical stress as an indirect verification of the role of hot phonons. The impact of hot phonon lifetime in

current degradation of InAlN/AlN/GaN HFET was reported earlier by applying high-field electrical stress. The lowest degradation of the drain current was obtained at the resonant 2DEG density of approximately $1 \times 10^{13} \text{ cm}^{-2}$, very close to the value of $9.3 \times 10^{12} \text{ cm}^{-2}$ which also coincided with the shortest signal delay time in a similar HFET at the same bias [¹⁰].

It is highly beneficial to expand the study using more sensitive measurement techniques such as low-frequency noise (LFN), which is particularly useful to address the mobility and trap-related fluctuations in an HFET channel and its vicinity [^{32,33}]. This may pave the way to further understand and identify the question: How and where does the trap generation occur in the HFET structure? In this report our goal is use the low-frequency phase-noise technique to monitor and verify the effect of the high-field electrical stress and its close relation to the hot-phonon lifetime as a function of the applied gate bias, and therefore the effective electron density in the channel.

For this aspect of the investigation, the InAlN/AlN/GaN structures were grown on sapphire substrates in a metalorganic chemical vapor deposition system. The structures consisted of a 250 nm AlN initiation layer grown at $\sim 1030^\circ\text{C}$, 3 μm of undoped GaN deposited at $\sim 1000^\circ\text{C}$, a 1 nm AlN spacer layer grown at 1000°C , a 20 nm $\text{In}_{0.15}\text{Al}_{0.85}\text{N}$ barrier layer grown at 800°C , and a 2 nm GaN cap layer grown at 900°C . The Ti/Al/Ni/Au ohmic contacts for the HFET devices were fabricated and mesa isolation was etched in a SAMCO inductively coupled plasma etcher based on Cl chemistry. Finally, the standard liftoff procedure was used to form the gate electrodes of Pt/Au (thickness 30/50 nm, length/width 2/90 μm).

The HFETs were selected for testing among nearly identical devices from the same wafer, based on their current densities, transfer properties, and leakage currents measured using the standard DC characterization methods. The maximum dispersion in the current density of the selected

devices was about 0.06 A/mm, which corresponds to a 5 % variation. The threshold voltage was about -6.8 V. The maximum 2DEG density of $2.3 \times 10^{13} \text{ cm}^{-2}$ was obtained from the Hall effect measurement; the minimum density was assumed to be zero at the pinch-off condition in biased HFETs. These two values and I_D vs. V_{GS} plots were used to estimate the sheet density as function of gate bias. All devices were subjected to a 7 hr DC stress at $V_{DS}=20 \text{ V}$ at different gate voltages.

Figure 21 (a) shows the change in the drain current, ΔI_D , after the electrical stress. Consistent with the earlier report [8], the minimum degradation took place at the gate voltage corresponding to the resonant 2DEG density of $9.2 \times 10^{12} \text{ cm}^{-2}$ where the change was below 20%, whereas a change as high as 77% (at zero gate bias) was observed in some samples at 2DEG densities far away from the resonance. **Figure 21 (b)** shows two representative HFETs that were stressed at resonant and off-resonant sheet density conditions. Off-resonant stress results exhibited some gate-lag (open circles) in addition to the severe drain-current drop compared with the devices stressed at resonant 2DEG condition (closed diamonds). We suggest the following account for these observations: The hot-phonon build-up under the off-resonance bias conditions causes both the drain-gate access region deterioration and trap generation in the barrier and buffer due to the thermally isolated subsystem of hot-electrons and hot-phonons [7].

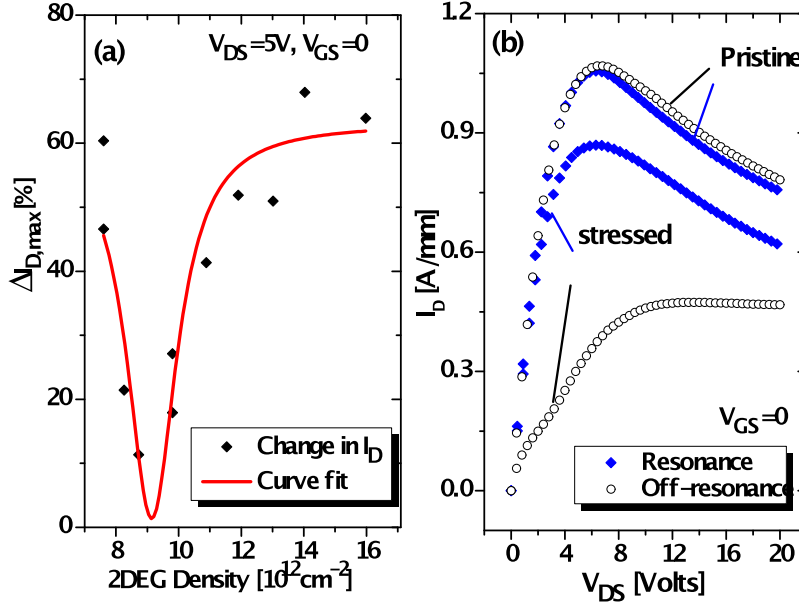


Figure 21. (a) Change in drain current ΔI_D vs. sheet density at $V_{DS} = 5 \text{ V}$ and the Lorentzian fit after 7 hrs of stress at $V_{DS} = 20 \text{ V}$; the minimum degradation occurs at a sheet density of $\sim 9.2 \times 10^{12} \text{ cm}^{-2}$. (b) Representative I_D vs. V_{DS} graphs at zero gate bias for two HFETs before and after the stress when the gate was biased to the hot phonon-plasmon resonance (closed diamonds) and at the off-resonance (open circles). The percentage of drain current degradation can be estimated from the ratio of the current after the stress (lower curve) to the value before the stress (corresponding upper curve).

We also monitored low-frequency phase noise for each device relative to a carrier signal at 4 GHz using an Agilent 5505 test set. More details regarding this particular technique can be found in Refs. [32-34]. After noting the least amount of degradation to be corresponding to the resonant 2DEG density, we obtained the change in the noise values from the data acquired in parallel with the DC measurements. In Figure 22, we show the change in noise at 1 kHz as a function of the 2DEG density estimated from varying gate biases. The trend in noise data followed exactly that of the ΔI_D data [(Figure 21 (a))] and a clear resonance at a sheet density around $9.6 \times 10^{12} \text{ cm}^{-2}$ was obtained from the peak-fit shown in Figure 22. This value is consistent with the values of $9.2 \times 10^{12} \text{ cm}^{-2}$ and $9.3 \times 10^{12} \text{ cm}^{-2}$ obtained from Figure 21 (a) and current-gain-cutoff-frequency measurements [8] at high fields, respectively. The reduction in the power output (ΔP_{out}) plotted

vs. 2DEG-density supports the noise data in that the minimum for power loss after stress for a given gate bias corresponds to the same optimal 2DEG density. As expected these high-field values are slightly larger compared to the 2DEG density ($\sim 6.5 \times 10^{12} \text{ cm}^{-2}$) acquired from the above mentioned direct hot-phonon lifetime results using microwave noise (2DEG) and Raman spectroscopy measurements (bulk) at low fields (see Figure 1). The reason for this difference is that the hot-electrons in GaN channel thermally spread over a larger volume and a higher 2DEG density is required to reach the resonance. It should also be noted that for gate biases larger than the value corresponding the optimal sheet density the drain current is lower and yet the degradation is worse. Details of low frequency noise measurements can be found later in this report. For lucidity, the degradation data as discerned by this technique are mentioned here.

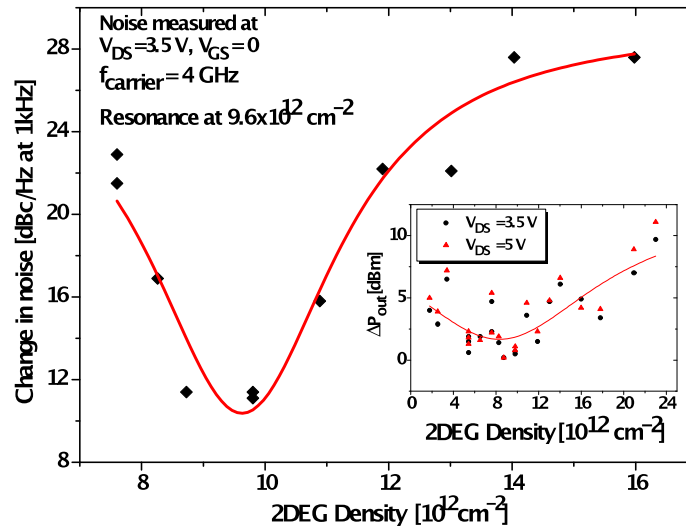


Figure 22. Increase in the noise measured at zero gate bias after 7 hr. electrical stress at 20V drain bias as a function of channel sheet density controlled by the gate bias. The clear resonance is observed at a sheet density around $9.6 \times 10^{12} \text{ cm}^{-2}$ from the peak fit (solid line), at which the degradation due to hot phonons is minimum. The inset shows the reduction in the output power after stress with a peak fit guiding the eye to see the trend. Output power was directly measured by feeding the device output into the spectrum analyzer.

Indeed the low-frequency noise technique turned out to be very a sensitive diagnostic tool for both mobility and number fluctuations in the channel of a device and offers valuable information for trap activity/analysis [^{32,35}]. The devices exhibited dramatically higher noise values varying from 11 dBc/Hz to 28 dBc/Hz after being subjected to the above mentioned stress conditions at $V_{GS}=-4V$ and $V_{GS}=-2.5V$, respectively. On the other side of the resonance, the noise increase was up to 25 dBc/Hz at $V_{GS}=-5.5V$. Specifically, the HFETs stressed under completely off-resonant 2DEG densities exhibited up to 14-17 dB higher noise values corresponding to the left and the right sides of the resonance, respectively, compared to those stressed at the resonant condition. These results combined with the data in **Figure 21 (b)** suggest that either number or mobility fluctuations or both contribute to the degradation. At the resonant-2DEG condition, the deterioration of the GaN channel quality and mild deep-trap generation in the buffer layer can be responsible for the higher noise and stronger drain-current drop [³⁶]. However, under the off-resonance conditions, up to 17 dB increase in noise-change is caused by carrier number fluctuation as a result of trap generation in the barrier and buffer layers as well as the amplified mobility-fluctuations due to the damage in GaN-channel. In this context, the current transient spectroscopy measurements were also performed on pristine and highly degraded devices at 430K for up to 5 ms pulse durations. Drain current was almost totally lost in degraded HFETs as opposed to a very small drop for pristine devices and no recovery observed for both indicating generation of deep traps in GaN buffer. In addition, a permanent loss in the drain current caused by stress implies that the channel degradation is likely. Further measurements and analyses are warranted to shed additional light on this matter such as photoionization of possible deep traps in buffer layer [³⁷] and change in channel resistance due to degradation.

To summarize this particular section, low-frequency noise measurements on InAlN/AlN/GaN HFETs showed that degradation due to high-field stress is 14-17 dB lower at a resonant sheet density of $9.6 \times 10^{12} \text{ cm}^{-2}$ compared with those degraded at off-resonant conditions. This 2DEG density value is consistent with the results from the current-gain-cutoff-frequency measurements and the effect of electrical stress on drain-current. The relatively small increase in noise at resonant condition after stress is attributed to the mild damage of the channel, whereas at off-resonant conditions, the additional noise is believed to be caused by the generation of barrier traps and damage to the channel itself. The results are consistent with the phenomenon of hot-phonon build-up and corresponding sheet density for ultrafast decay due to the phonon-plasmon coupling.

Degradation and Field-assisted emission in HFETs using low-frequency noise technique

We utilized low-frequency noise measurements to probe electron capture and emission from the traps in AlGaIn/GaN HFETs as a function of drain bias. The excess noise-spectra due to generation-recombination effect shifted higher in frequency with the elevated temperature from room temperature up to 446 K. These temperature dependent noise measurements were carried out for four different drain-bias values from 4 V up to 16 V with 4 V increments. The shift of the excess-noise in frequency was also seen with increasing drain bias. The characteristic recharging times for the trapped electrons varied within the range of 26 μs - 32 ms for the highest and lowest values of the drain voltage and temperature used in the experiment, respectively. The activation energies of the traps corresponding to the four different voltage values were extracted using temperature dependence by Arrhenius analysis. The trap energy at zero drain-bias was obtained

as 0.71 eV by the extrapolation technique. This result suggests that the LFN is a very sensitive diagnostic tool to characterize trap states.

To reiterate GaN based HFETs exhibit remarkable performance in high frequency and high power applications [1]. However, the presence of electronic traps in the device structure is still a major problem and limits its performance and reliability [38]. Several techniques, such as deep-level transient spectroscopy [39,40,41,42], low-frequency transconductance dispersion [43,44], pulsed current transient spectroscopy [45,46], and photoionization spectroscopy [47,48] as well as the standard transient current-voltage and capacitance-voltage methods [49], have been used to identify these traps, their spatial locations and the effects on the device performance. Analyses of these traps can be assuaged some by bringing to bear new tools. For example, the pulsed current-transient spectroscopy technique is not sensitive to shallow traps if the buffer layer suffers from the deep traps, for which the transient current recovery is too long. Thus, it is beneficial to implement more sensitive and versatile measurement techniques to monitor and characterize the charge traps in the HFET structure.

Low-frequency noise (LFN) spectra [50,51], particularly those originating from generation-recombination (GR) processes [52,53], are beneficial for analyzing semiconductor quality for both interface and bulk properties owing to the fluctuations in the channel-current being affected by capturing and emission of the electrons [54,55].

In this work, we show that a specific LFN, measured with an integrated residual phase-noise setup, is able to detect the additive noise contribution to find the activation energy of a dominant GR-noise yielding defect(s) at various drain bias values. Using the activation energy values of

the traps extracted from the temperature-dependent measurements corresponding to each bias condition, we obtained the dominant trap energy level at zero applied drain bias.

We carried out the noise measurements using an Agilent E5505A test-set with a built-in phase detector (mixer) [Figure 23]. Setting the input ports of the mixer 90 degrees out of phase, we measured the residual phase fluctuations of the HFETs at certain bias conditions. The single-sided-spur calibration technique was used to achieve the maximum sensitivity using an extra signal generator. The main difference between our technique and the baseband method [^{53,56}] is simply the application of high-frequency carrier signal. We applied a 4 GHz signal with an input power of approximately 1 mW and monitored the single-sideband low-frequency response within a 100 MHz offset frequency. We noted the corner frequencies spanning up to 1 MHz using the residual phase-noise technique. The corner frequencies observed using baseband method were about two orders of magnitude lower than the ones observed using the phase-noise technique at identical bias conditions. This allowed us to observe the noise levels below the noise floor afforded by the baseband method [⁵⁷].

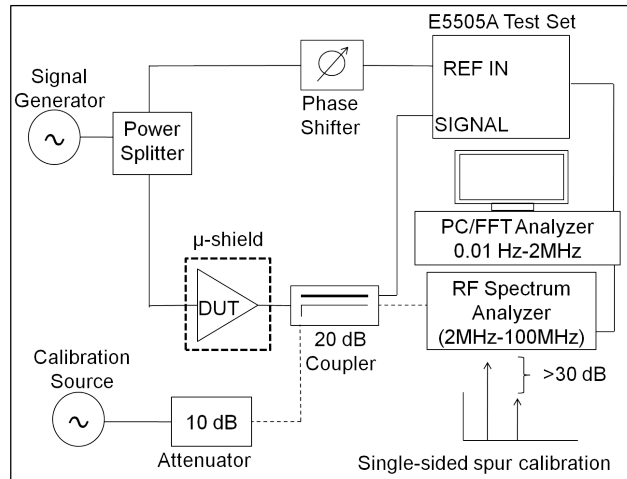


Figure 23. Block diagram of the Agilent E5505 residual phase-noise measurement setup with the single-sided spur calibration technique.

HFET PARAMETERS AND DC RESULTS

The test HFET structures to be characterized were grown on sapphire by metalorganic chemical vapor deposition (MOCVD). A 2.5- μm -thick undoped GaN buffer was deposited following a 250-nm-thick AlN initiation layer on sapphire. Next, a 20-nm-thick AlGaN barrier layer was grown with 25% Al mole fraction. The Hall-effect measurements yielded a sheet carrier density $n_s \approx 1.2 \times 10^{13} \text{ cm}^{-2}$ and an electron mobility $\mu_e \approx 960 \text{ cm}^2/\text{Vs}$ at room temperature. Figure 24 (a) and (b) show the schematic diagrams of the HFET structure with the metal contacts and the conduction band of the buffer and the barrier. The typical I_D vs. V_{DS} family output curves for the HFETs are shown in Figure 24 (c). Figure 24 (d) shows the transfer properties of the HFETs with a maximum transconductance of 230 mS/mm and a maximum drain current of 520 mA/mm at $V_{GS}=0$. The devices exhibited $1.0 \times 10^{-4} \text{ A/mm}$ gate leakage at $V_{GS} = -8 \text{ V}$ and a pinch-off voltage of -2.9 V.

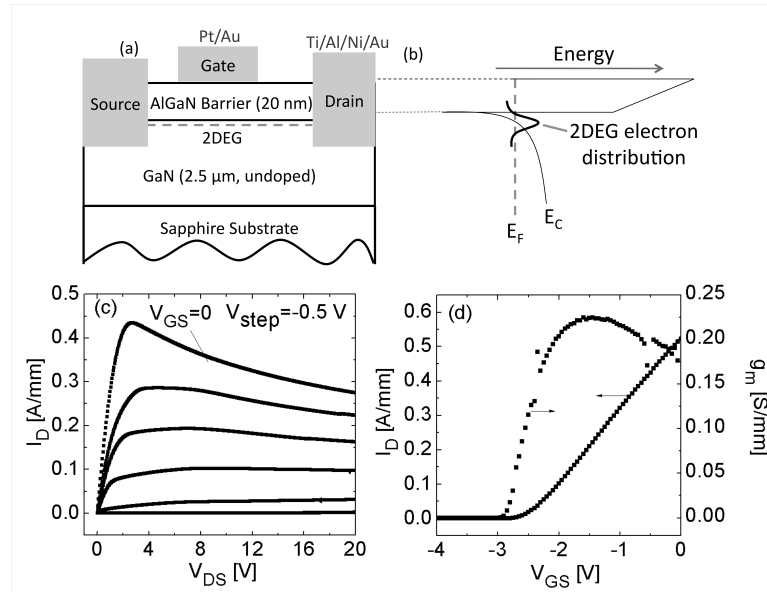


Figure 24. (a) A top-down schematic diagram of the HFET layer structure with the ohmic and Schottky contacts. (b) The schematic conduction band diagram of the barrier and the buffer layers with the 2DEG distribution. (c) The I_D vs. V_{DS} family of curves for the HFETs is seen with the increments of V_{GS} by -0.5 V. (d) Transfer properties of the HFET devices.

LFN RESULTS AND DISCUSSION

The LFN measurements consistently manifested a broad additive-noise peak, which could be attributed to the generation-recombination (GR) noise arising from a definite trap level in the barrier or interface [Figure 25]. This shows that the noise technique we used is sensitive to the trap-originated variations in the channel-noise spectra of the devices. The GR noise in an HFET originates from traps that randomly capture and emit electrons, thereby causing fluctuations in the number of electrons which carry current in the channel. The spectrum has two main components with one or more Lorentzians in addition to the $1/f$ background. Thus, the noise-spectral-density (NSD) has the form of [53]:

$$\text{NSD} = \frac{A}{f^\gamma} + \sum_i \frac{B_i \tau_i}{1 + (2\pi f)^2 \tau_i^2},$$

Equation 4

where τ_i are the time constants associated with the abovementioned transitions and γ is a parameter close to 1. A and B_i are the coefficients characterizing the crystal quality, trap concentration and number of electrons in the channel.

Trapping and detrapping are processes that have strong lattice-temperature dependence. Thus, an analysis of the position of the broad GR peaks in Figure 25 with respect to temperature would allow us to extract the activation energy of the traps (Equation 5). In order to achieve this, we acquired the data from room temperature up to 446 K, and noted the shift of the peaks towards higher frequencies with increasing temperature. We fit the peaks to a Lorentzian function

according to Equation 4 following the subtraction of the $1/f$ background from the GR spectra [52]. This allowed us to obtain the time constant for a certain temperature. Using the acquired trap characteristic times, the energy level of the traps can be found from the equation

$$\tau_T = \tau_0 \exp(E_T/kT),$$

Equation 5

where τ_T is the trap time constant, E_T is the trap energy level below the conduction band, k is the Boltzmann constant. From the definition of Shockley-Read density, τ_0 is equal to $(v_n \sigma_T N_c)^{-1}$, where $v_n \propto T^{1/2}$ is the average drift velocity of the electrons, σ_T is the capture cross section of the traps, and $N_c \propto T^{3/2}$ is the density of states in the conduction band [53,58].

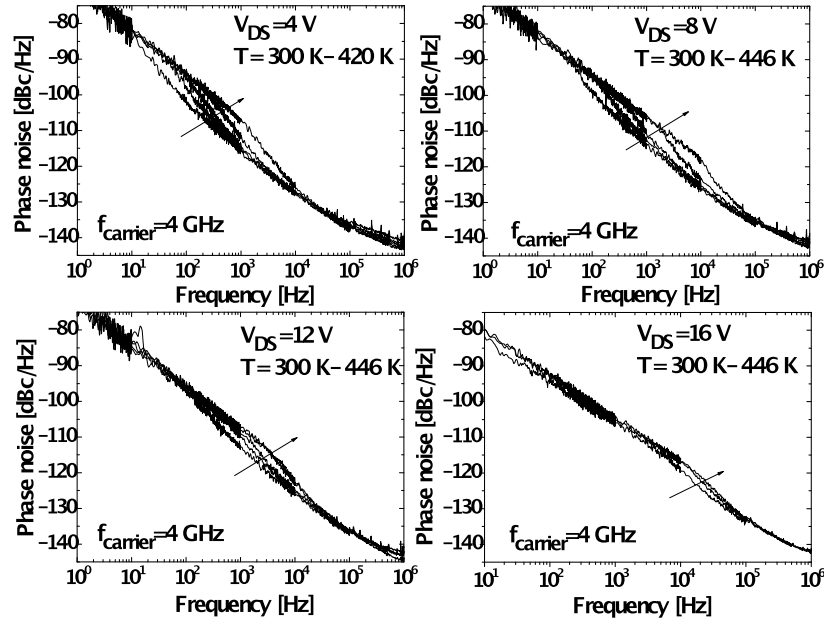


Figure 25. Four sets of noise-spectral-density curves at V_{DS} values from 4 V to 16 V within the indicated temperature ranges. The arrows show that the spectra shift higher in frequency with both increasing drain bias and temperature. The trap time constants vary from 0.1ms to 32 ms for $V_{DS}=4$ V and from 30 μ s to 1.6 ms for $V_{DS}=12$ V. The broad Lorentzian feature of the spectra is predominantly due to the non-uniform electric field in the AlGaN barrier region and variation in the trap barrier heights within the barrier or surface.

The behavior of the additive GR contributed noise spectra at different drain bias conditions must be analyzed carefully to understand the physical mechanisms involved, which leads to spectrum shifts in the frequency axis. Hence, we can draw more conclusions related to the trap characteristics within the context of emission and capture processes. The activation energy E_A acquired from the Arrhenius analysis is the amount of energy to excite the localized electrons confined in the potential barrier of the traps to the conduction band at certain bias conditions. The deeper potential barrier results in larger activation energy with respect to the bottom of the conduction band and longer time constants according to Equation 5. The trap potential barrier is skewed in the presence of an external electric field, which decreases the effective trap barrier in the opposite direction of the field vector for a hydrogen-like potential well. This case is important for GaN based HFETs since there is a large external electric field in the barrier of the structure due to the applied drain-source bias. Naturally then we now turn our attention the effect of external electric field on the emission rates and on the lowering of the activation energy.

In the presence of a strong electric field, the effective trap potential barrier height can decrease remarkably, and consequently this increases the emission probability of the trapped electrons. This effect is known as the Frenkel-Poole effect and for a singly charged center the lowering of the potential barrier can be characterized as follows [1]:

$$\Delta\phi_{FP} = \left(q^3 / \pi \epsilon_0 \epsilon_r \right)^{1/2} F^{1/2},$$

Equation 6

where q is the elementary electron charge, $\epsilon_0\epsilon_r$ is the dielectric constant of the crystal, and F is the magnitude of the external electric field. Hence, we can rewrite Equation 5 including the field dependency as

$$e(T, F) = AT^2 \exp\left[-(E_T - \Delta\phi_{FP})/kT\right],$$

Equation 7

where $e(T, F)$ is the emission rate of the electrons and A is a field dependent pre-exponential factor. The field-dependent activation energy, $E_A(F)$, can be defined as the difference between the trap energy and the barrier lowering:

$$E_A(F) = E_A(0) - \Delta\phi_{FP} = E_T - \left(q^3 / \pi\epsilon_0\epsilon_r\right)^{1/2} F^{1/2},$$

Equation 8

where $E_A(0) = E_T$ is the binding energy of the trapped electrons at $F = 0$. Knowing that the electric field is directly proportional to the applied voltage in continuous media, Equation 8 gives:

$$E_A(V_{DS}) = E_T - \beta V_{DS}^{1/2},$$

Equation 9

where β is a constant.

In [Figure 25](#), we show the noise spectra for four different drain bias values. The noise spectra shift higher in frequency with the increasing temperature and drain-source bias as expected. The GR features monitored in the LFN spectra are broader and weaker than the data shown in [Ref. 52](#) partly stemming from the traps experiencing the non-uniform electric field in the barrier layer, where the electric field is at its maximum value on the drain side of the gate [\[1\]](#). Additionally, the broadening could also be caused by the trap barrier-height variation within the surface or the AlGaIn barrier. Moreover, the weakening of the distinct GR spectrum can be attributed to the lower concentration of the traps with a certain time constant leading to the GR excess-noise.

Assuming that the electron emission above room temperature dominated by the Frenkel-Poole mechanism in the AlGaIn barrier, we extracted the zero-field trap activation energy, E_T , using the following method [\[45, 59\]](#). First we measured the temperature dependent LFN for a device with 1 μs gate length for four different drain-source bias conditions within the range of 4-16 V with 4 V increment to verify the validity of the FP model. All the measurements were performed at zero gate bias. Then we obtained the emission rates for each LFN spectrum from the additional Lorentzian characteristics of the spectra [\[Figure 25\]](#) [\[60\]](#). The temperature and drain-bias dependent emission rates exhibited a wide range of values. The characteristic trap time constants calculated from these emission rates varied about three orders of magnitude within the range of 32 ms- 26 μs for the temperature and bias values at (300 K, 4 V) and (446 K, 16 V), respectively.

We extracted the activation energy for each bias condition from temperature dependence using the Arrhenius analysis [\[Figure 26\]](#). The activation energy is simply the slope of the $\ln(\tau T^2)$ vs. $1/kT$ plot for a certain drain bias in units of eV ([Equation 5](#)). The trap energies were found as 0.44 eV, 0.33 eV, 0.25 eV, and 0.17 eV corresponding to the V_{DS} = (4 V, 8 V, 12 V, and 16 V),

respectively. Figure 26 shows the Arrhenius plots at each bias condition and the corresponding activation energy values. The zero-bias binding energy is given as 0.71 eV in Figure 27 by extrapolation, which is 0.27 eV lower than the activation energy at $V_{DS}=4$ V. It is obtained from the fit to the plot $E_A(V_{DS})$ vs. $V_{DS}^{1/2}$ according to Equation 9. This confirms that there is a substantial barrier lowering due to the external bias.

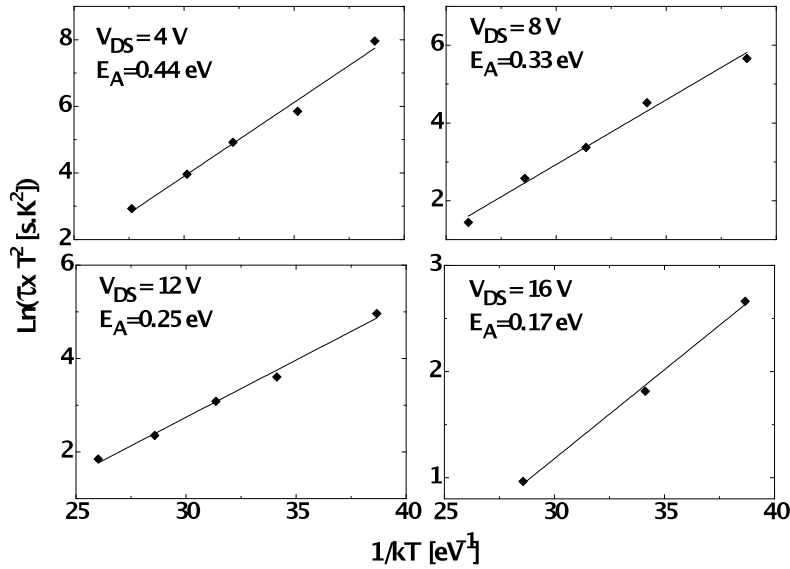


Figure 26. The Arrhenius plots for all drain-source bias values for which the temperature dependent low-frequency noise (LFN) measured. The plot at $V_{DS}=16$ V has only three data points since it is hard to extract the emission rates at the highest applied values of drain-bias and temperature combination.

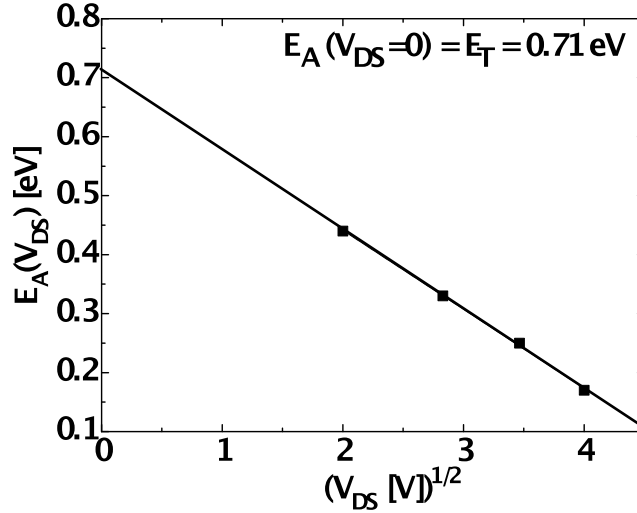


Figure 27. Linear fit for the activation energy vs. $(V_{DS})^{1/2}$ plot [Eq. (6)]. Trap energy at zero bias can be extracted from the y-intercept as 0.71 eV.

The dominant GR contribution to the noise spectra may arise spatially from the regions close by the channel. The additive feature of the GR noise has been investigated in detail in [Reference 51](#). According to the number fluctuation theory, a uniformly distributed trap concentration in the barrier layer causes the $1/f$ noise in an HFET. The deviation from the $1/f$ noise with a certain GR feature in the noise spectra obtained here implies that the trap concentration in the close vicinity of the channel is not uniform. This effect is important in terms of the device reliability and performance which may cause generation of more traps under electrical stress.

In short we employed LFN measurements for AlGaIn/GaN HFETs and monitored the evolution of the channel-noise spectra as a function of drain-source bias in order to probe the trap characteristics. The activation energy at each bias point is obtained from the temperature dependence of the emission using Arrhenius analysis. The trap energy at zero-bias was extracted as 0.71 eV by extrapolation technique. The activation energy at a drain bias of 4V was 0.44 eV. This validated that the barrier lowering due to the field-assisted emission (Frenkel-Poole effect)

in the barrier layer is substantial. The non-uniform external field in the barrier layer causes the additive GR spectrum to have a broader feature. The dominant trap effect monitored here can arise from the regions in the vicinity of the channel. The results show that the LFN is a very sensitive and useful diagnostic tool to characterize the trap states in the AlGaIn/GaN HFETs.

The effect of hot electrons and hot phonons on the degradation of HFETs was studied with four point stress measurements which included high drain voltage near pinchoff which probes the effect of hot electrons and high drain voltage with high current which probes the effect of hot electrons/hot phonons/ temperature. The partial effect of temperature can be extracted by biasing the device to high current but low drain bias. In this context $\text{In}_{15.7\%}\text{Al}_{84.3\%}\text{N}/\text{AlN}/\text{GaN}$ Heterojunction Field Effect Transistors (HFETs) have been electrically stressed under four different bias conditions: on-state-low-field stress, reverse-gate-bias stress, off-state-high-field stress, and on-state-high-field stress, in an effort to elaborate on hot electron/phonon and thermal effects. DC current and phase noise have been measured before and after the stress. The possible location of the failures as well as their influence on the electrical properties has been identified. Results show that reverse-gate-bias stress causes trap generation around the gate area near the surface, which has indirect influence on the channel. While off-state-high-field stress and on-state-high-field stress induce deterioration of the channel, which causes directly reduction of drain current and increase of phase noise. The channel degradation is ascribed to the hot-electron and hot-phonon effects.

The four bias points employed here are (i) on-state-low-field stress ($V_{GS} = 0$ V, $V_{DS} = 6$ V), (ii) reverse-gate-bias stress ($V_{GS} = -20$ V, $V_{DS} = 0$ V), (iii) off-state-high-field stress ($V_{GS} = -10$ V, $V_{DS} = 20$ V), and (iv) on-state-high-field stress ($V_{GS} = 0$ V, $V_{DS} = 20$ V). An ensemble of the HFET devices on the same wafer has been studied, and the results from a representative device for each bias point are presented here. Each stress test started with an initial 5 hour stress, and then followed by another 20 hour stress. The dc transfer characteristics and phase noise were measured before and one day after each stress test. If there were any shifts of pinch-off voltage (V_{th}), the transfer characteristics were adjusted by an amount equaling the shift of V_{th} . The noise-spectra-density (NSD) of HFETs can be expressed as in Equation 4.

The results for the on-state-low-field stress are demonstrated in Figure 28, where the NSD shows a $1/f^\gamma$ shape. The extracted Hooge parameters were on the order of 10^{-4} , which are comparable to AlGaIn/GaN based HFETs. The change in NSD was not discernible even after 25 hours of stress, and the drain current shows little change as well. The effects due to the reverse-gate-bias stress are illustrated in Figure 29. The drain current showed little change for the first 5 hour stress and $\sim 5\%$ change after the 25 hour stress (Figure 29 (a)). A double peak feature appeared in the g_m plot after 5 hours of stress and became more apparent after the 25 hour stress. This effect is very similar to the kink effect usually ascribed to hot-electron injection into donor-like traps followed by subsequent field-assisted de-trapping under high electric field¹¹. Thus, most likely the hot-electron induced trap-generation occurred in the barrier layer as expected since only the gate area was affected under corresponding stress condition. The influence was also observed in the noise measurement as demonstrated in Figure 29 (b), where the G–R peak below 1 kHz in the pristine devices diminished after 25 hour stress. A plausible explanation can be ascribed as

follows: deep traps were generated during the stress around the gate area, they rendered the pre-existing shallow donor-like traps inaccessible for electrons and caused the observed reduction of the G–R peak intensity in NSD below 1 kHz. The created deep traps should be temporarily stable or equivalently have a very large time constant, thus would not be reflected in the NSD spectrum which covers from 1 Hz to 100 kHz. For frequencies not influenced by this G–R peak, i.e. above 1 kHz, the NSD remained the same, which meant that the A parameter in Equation 4 does not change under the reverse-gate-bias stress condition.

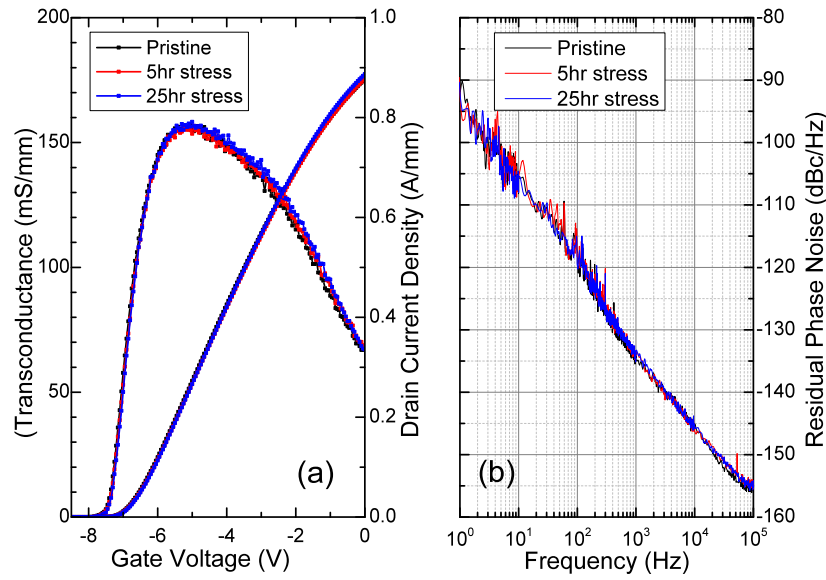


Figure 28. Effect of on-state low-field stress on (a) I-V and transconductance measured at $V_{DS}=6$ V; (b) phase noise measured at $V_{GS}=0$ V, $V_{DS}=6$ V

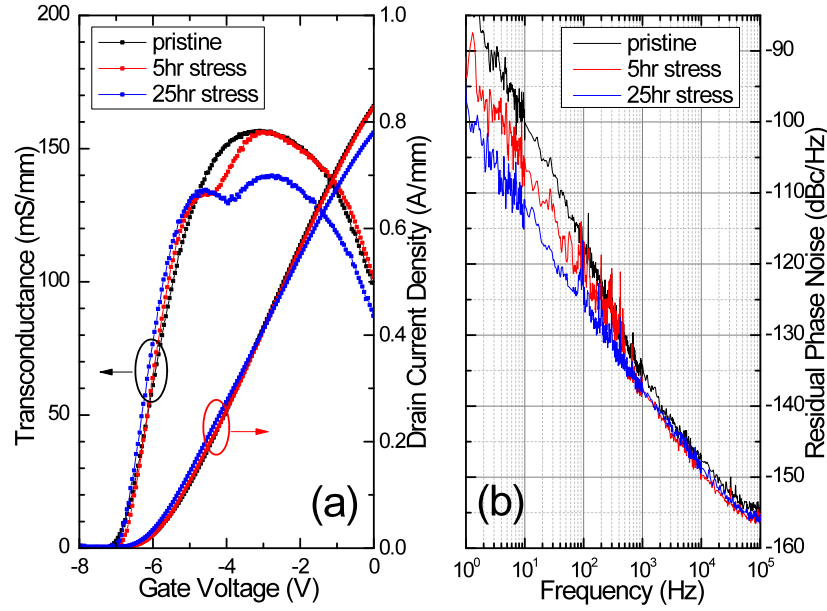


Figure 29. Effect of reverse gate bias stress on (a) I-V and transconductance measured at $V_{DS}=6$ V; (b) phase noise measured at $V_{GS}=0$ V, $V_{DS}=6$ V

In contrast to the above two stress conditions, the off-state-high-field stress exhibited a noticeable reduction in the drain current and an increase in NSD (Figure 30). And the most damaging stress condition is the on-state-high-field stress as demonstrated in Figure 31, where the drain current permanently decreased to $\sim 25\%$ of the original value and the NSD increased by about 25-30 dBc/Hz after the 25 hour stress. One common feature for these two stress condition is that the g_m degradation is most pronounced near the g_m peak rather than at high V_{gs} bias points (i.e., with high drain current), thus the major degradation is associated with the decrease of channel conductivity instead of the increase in the drain access resistance R_D caused by the electron trapping in the gate-drain access region. This assertion is consistent with the change of channel resistance R_{Ch} and drain access resistance R_D after stress, where the increase of R_{Ch} takes around 70% of the total increase of source-drain resistance (The method for the resistance measurement).

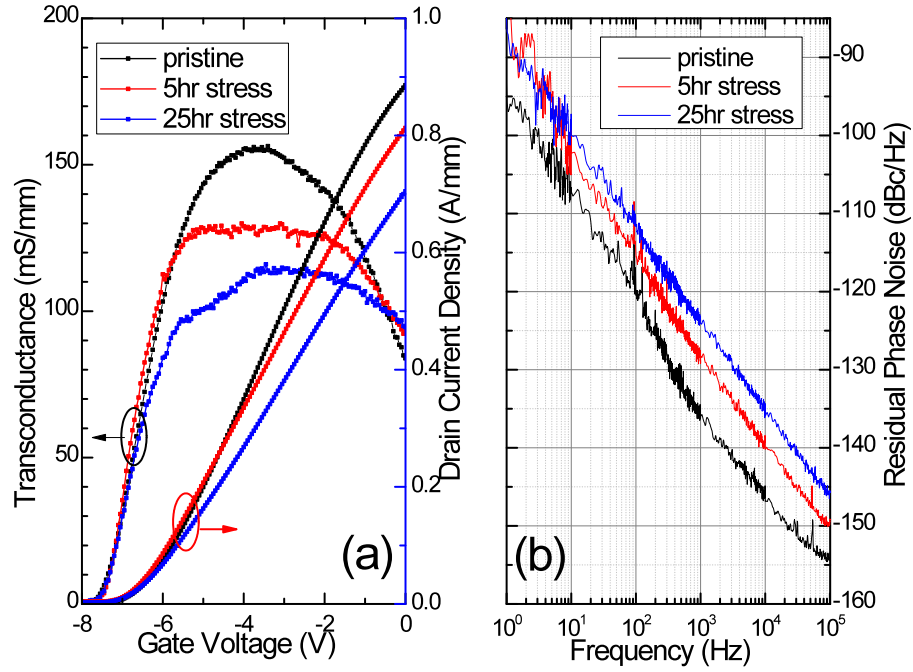


Figure 30. Effect of off-state high-field stress on (a) I-V and transconductance measured at $V_{DS}=6$ V; (b) phase noise measured at $V_{GS}=0$ V, $V_{DS}=6$ V

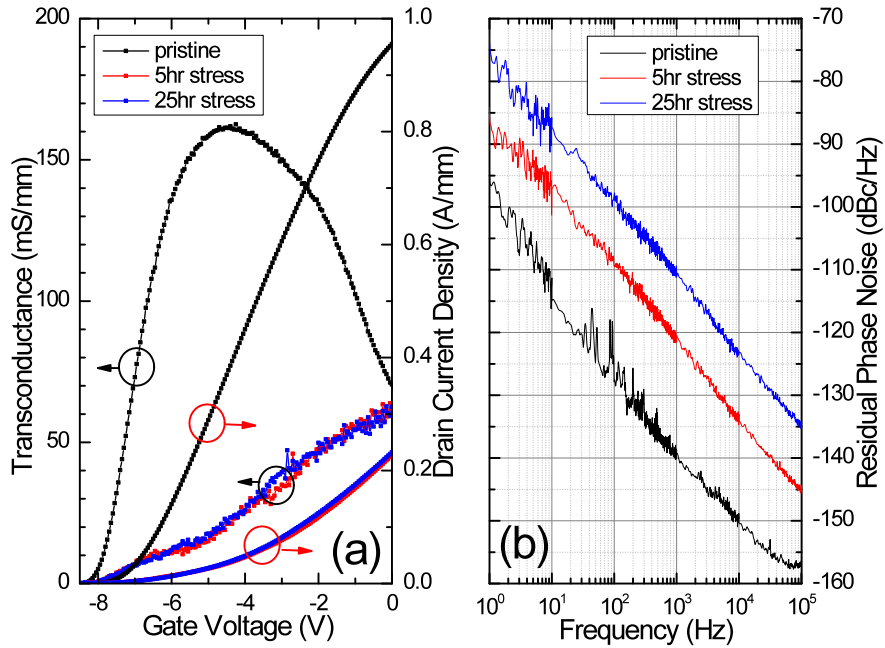


Figure 31. Effect of on-state high field stress on (a) I-V and transconductance measured at $V_{DS}=6$ V; (b) phase noise measured at $V_{GS}=0$ V, $V_{DS}=6$ V

The results of **Figure 28** demonstrated that the electrical properties of the devices show no change after the on-state-low-field stress. Consequently, the channel self-heating effect due to the drain current at moderate drain bias is not likely to cause any degradation in the channel. The device temperature under on-state-high-field stress is expected to be around 200°C higher than that under the on-state-low-field stress if use a thermal resistance of around 25 °C •mm/W¹⁵. In order to isolate the self-heating effect from the on-state-high-field stress, an ensemble of pristine devices were stressed under on-state-low-field stress at 200°C to test the heating effect only. No permanent degradation of drain current was observed, which is consistent with the good thermal reliability of InAlN/GaN based HFETs. Thus, the large degradation under on-state-high-field stress cannot be attributed to the self-heating effect only. The reverse-gate-bias stress and the associated piezoelectric effect can cause damage to the barrier layer and change the drain current by depleting the 2-dimensional-electron-gas (2DEG) in the channel. However, the change in the drain current predominantly results from a shift of the pinch-off voltage in our experiments. Indeed, **Figure 29 (a)** demonstrates a very small change in the drain current after correcting for the pinch-off voltage. Thus, the degradation is limited to the barrier layer, and moreover, most probably near the surface area far away from the channel, which has only indirect influence on the channel. This assertion is plausible since remote ionized impurity scattering will cause minor effect on the mobility of the 2DEG for a typical barrier thickness of 20 nm, particularly at room temperature and above. This is also confirmed by the NSD results since the A parameter shows no change after the reverse gate bias stress as discussed above.

The degradation of drain current and NSD caused by the off-state-high-field stress should directly be induced by the electrons leaking through the channel. Due to the high source–drain

voltage, these electrons are hot and can cause direct damage in the channel, i.e. through the generation of trap states in the channel. This in turn causes a reduction of channel conductivity and increase of the NSD. This is also consistent with the high degradation rate for the on-state-high-field stress considering the large amount of the hot-electrons in the channel compared to that of the off-state-high-field stress condition. Also the large amount of hot-electrons in the channel will induce large density of hot phonons and the resultant strong hot-phonon effect, which can further speed up the degradation. The increase of the A parameter in the NSD exclusively correlated with the reduction of the drain current as demonstrated by the on-state-high-field and off-stat-high-field stress, thus the increase of noise should directly relates to the increase of R_{CH} and/or increase of R_D by electron trapping in the gate-drain access region. Considering the A parameter in NSD didn't change after reverse-gate-bias stress, the increase of noise under off-state-high-field stress and on-state-high-field stress most likely comes from the increase of R_{CH} due to the channel degradation instead of the increase of R_D .

CONCLUSIONS:

In this reporting period, we firmly established that the hot LO phonon decay goes through a minimum with respect to the electron density, minimum always occurring at the density for which the plasmon frequency and LO phonon frequency resonate. When converted to sheet density, the resonance point could be shifted to higher sheet densities by electrically heating the electrons. Experiments involving FET degradation, carrier velocity as determined by the transit time under the gate which in turn was determined by the current gain cut off frequency. The same was also noted conspicuously and in the change in low frequency noise which shows a

minimum at this resonance as well. Prominently, all the aforementioned observations are uniformly consistent in that the device degradation is minimum at the above mentioned resonance, the cut off frequency and thus the carrier velocity is the highest at the same resonance, and the change in the low frequency noise which is sensitive to traps is the minimum at the same resonance which is when the LO phonon and plasmon, for the particular carrier concentration, energies match.

These investigations shed the much needed new light on the topic in that LA phonon consideration, which are commonly held and defended fiercely, is NOT the only deterministic parameter that should be considered in the realm of heat removal from FET channels. Our studies firmly demonstrate and assert that LO phonon decay to LA phonon is the bottleneck mechanism and that devices should be operated at or near the resonance for efficient heat removal and thus reduced damage under operation. Furthermore, the aforementioned efficient LO phonon decay bodes well for carrier transport as well due to reduced scatterers at high fields which is manifested by minimum electron transit time under the gate. As discussed, to expand optimum device operation regime to high carrier densities, we begin to undertake investigations of a camel back like dual channel structure, in terms of vertical electron distribution. We must underscore again, once the hot electron energy is transferred to LA phonons through the route of LO- LA phonon decay, one can then begin considering the impact of thermal conductivity which is governed by LA phonon propagation. Our effort confirms what should be known, but is often not, which is that insightful investigation and determination of the underlying physics invariably lead to uncovering the critical processes taking place which then pave the way for effective solutions.

Publications resulting from this work

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